Multi-level Methodology for CMOS SOI/SOS MOSFET Parameterization for IC Radiation Hardness Simulation with SPICE

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Abstract

The multi-level methodology for CMOS SOI/SOS IC element parameterization for VLSI radiation hardness prediction by CAD systems is developed.

The methodology includes semiconductor technology simulation, CMOS SOI/SOS MOSFET device simulation with radiation effects, irradiated test structures investigation, radiation dependent SPICE model parameter extraction with ICCAP. The measured data of irradiated MOSFET test structures is used for TCAD calibration and SPICE model creation. The results show a good correlation between the simulated with the developed models and measured IC and VLSI response to the total dose and other components of the radiation environment.

1. Introduction

SOI/SOS CMOS technologies are promising new possibilities for LSI and VLSI radiation hard applications in space, military and other special systems. The advantages of dielectric isolation are well known: very good individual electrical isolation of devices, low levels of leakage current, freedom from latch-up, higher packing density, reduced junction capacitance.

However, the radiation characterization and associated hardness assurance testing of ICs and complex logic VLSI can pose significant cost and schedule problems for most of space and special programs. Often fully functional circuits cannot be obtained for radiation testing during the initial phase of a design program. In this case the adequate methodology is necessary to generate model libraries for prediction of the IC and VLSI behavior in the radiation environment. The key points of the described methodology is thorough approach from IC manufacturing simulation to MOSFET parameterization, including irradiated test structures research.

In work [2] the special software tool BERT was used to generate MOSFET SPICE model parameters for radiation environment. The approach is effective for circuit simulation but it needs very large volume of measured data and can not be applied to estimate transistor parameters before chip manufacturing. So it is not possible to iterate an improved design changing the transistor technology, geometry and layout to enhance the radiation hardness.

This paper describes improved multi-level methodology with additional TCAD stage for transistor characteristic simulation with accounting the radiation effects. The separate parts of the methodology were presented previously [2-5,7].

The developed multi-level methodology is shown in the flow chart in Fig. 1. It includes the next simulation levels.

1.1. SOI/SOS CMOS technology simulation level

The first level in the methodology is CMOS SOI/SOS manufacturing simulation with Sentaurus TCAD tool. The input data is usual CMOS SOI or SOS IC manufacturing process description and output data – the simulated structure of a SOI/SOS MOSFET. This level is traditional and doesn’t have any features.

1.2. SOI/SOS MOSFET structure TCAD simulation level

`The second step in the methodology is to simulate the SOI/SOS MOSFET structures (result of the first level) and to produce MOSFET static and dynamic characteristics. The feature of this level in

comparison with traditional design process – the account of radiation effects in Sentaurus TCAD tool. Total dose, pulse irradiation and heavy ion strike effects on MOSFET structures are simulated at this level. We have modified TCAD tool by including radiation effects which have not been accounted earlier.

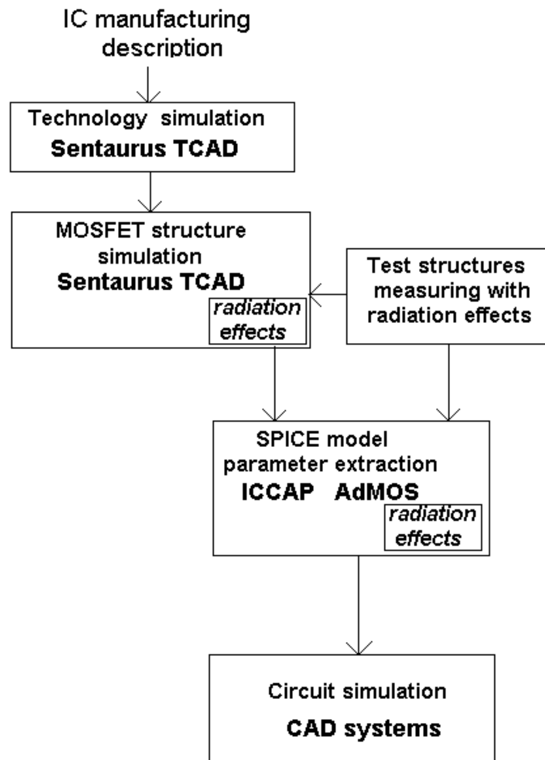

Fig. 1 The flow chart of the developed multi-level methodology

Sentaurus TCAD built in model for total dose allows to simulate MOSFET device characteristic shift only due to charge of holes trapped in oxide regions. To extend TCAD possibilities we have added the additional model to TCAD [5]. The proposed modeling technique [5] takes into account the effects of carrier mobility degradation and interface traps generation due to radiation.

In general, the modified TCAD tool provides more correct simulation of a total dose, pulse irradiation and heavy ion strike effects [5] on SOI/SOS MOSFETs. So it is possible to estimate SOI device radiation hardness before their production.

2D, 3D, Quasi 3D –modeling techniques are used depending on SOI/SOS MOSFET structure/layout features. As soon as the methodology was developed for radiation hardened VLSI design, the modeling technique depends on kind of special MOSFET layouts, presented in Fig. 2 [6].

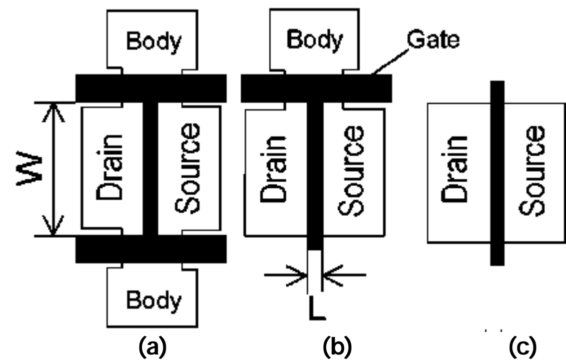

Fig. 2. Radiation hardened MOSFET layouts: (a) H-shape gate, (b) T-shape gate, (c) I-shape gate [6].

Complete, but time expensive 3D modeling technique is used for detailed simulation of radiation hardened SOI MOS structures with possible side leakage currents: I- and T- shape gates in Fig. 2.

Simple 2D modeling (along the MOSFET channel) approach is used for structures which have not side leakage currents after irradiation: H-shape gate (see Fig. 2), for example.

Quasi 3D modeling technique, developed by us [5] is used for investigating and estimating of leakage currents in conventional structures (I-shape gate in Fig.2).

Comparison of 2D and quasi 3D simulated Id=f(Vgs) characteristics of 0.5 um SOI nMOS for different doses was presented at [5].

Important aspect of the level is TCAD calibration by comparison the simulated characteristics of irradiated MOSFETs with the measured ones. The coefficients of radiation dependences are tuned to provide fitting of simulated I-V-curves to the measured ones.

1.3. Investigation of SOI CMOS test structure behavior in radiation environment

Standard SOI CMOS test transistor geometries are selected to represent transistor variations in real chip. MOSFET characteristics are measured for different total dose values (X-rays are usually used due to simplicity) and heavy ion fluence. MOSFET I-V-and C-V-characteristics are measured. The changes in characteristics: threshold voltage, mobility, leakage current, switching and dynamic characteristics due to the radiation environment conditions in n- and p-channel SOI/SOS MOSFETs with different sizes are being investigated. The obtained characteristics are used then by two ways:

- for TCAD tool calibration (see earlier) and
- as input data for MOSFET SPICE model parameter extraction.

1.4. Parameter extraction of SPICE macro model for SOI/SOS MOSFETs

The developed macro model for SOI/SOS MOSFETs taking into account radiation effects is shown in Fig. 3. The model and parameter extraction process were described in details earlier [7].

The proper SOI MOSFET is described by BSIMSOI model with dose dependent parameters (*VTHO* for threshold voltage; *UO, UA, UB* for carrier mobility, *VOFF, NFACTOR* etc. for subthreshold slope).

$I_{ph}(t)$ are the time dependent current sources that account for the effects of ionizing radiation pulses or effects of heavy ion penetrating the transistor structure.

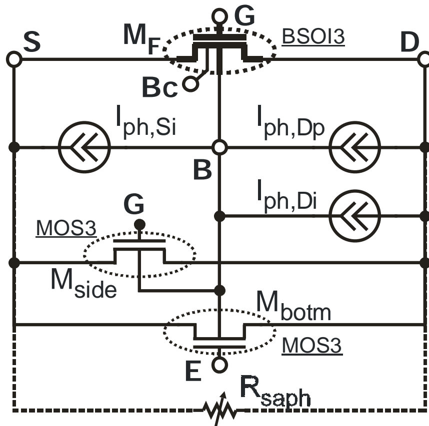

Fig. 3 . The macromodel for SOI/SOS MOSFETs taking into account the radiation effects [7].

Additional MOSFETs (M_{botm}, M_{side},) (MOS3 model with dose dependent parameters) are used to simulate the radiation-induced bottom and sidewall leakage currents in irradiated *SOI n-MOSFET*. It is seen that the gate of the bottom parasitic MOSFET is connected to the substrate of the SOI structure, the gate of the sidewall parasitic MOSFET is connected to the gate of the front-gate MOSFET. This feature allows to separate the sidewall and bottom currents for para,eter extraction purposes.

For MOSFET produced in "silicon an sapphire technology", a parasitic time dependent sapphire resistance $R_{saph}(t)$ is used to account for sapphire conductance during pulse irradiation. $R_{saph}(t)$ is activated pulse irradiation is modeled.

We used the macromodel approach by the following reasons:

1. It uses the well developed BSIMSOI model and allows the user to take into account the MOSFET radiation effects by a simple manner, and to involve any standard transistor-level simulator at his choice (no specialized simulator is required).
2. The macromodel approach doesn't require model modification to account radiation effects (which is not so simple).

If no leakage currents are observed, the macromodel is simplified to only front-gate MOSFET BSIMSOI model with dose dependent parameters.

All the macro model (Fig. 3) parameters are extracted with ICCAP software [8] with AdMOS block for BSIMSOI model from the set of I-V-characteristics $I_D=f(V_G, V_D, V_S, V_{SUB})$ and C-V-characteristics obtained by one of two possible ways:

- measured using irradiated SOI/SOS MOSFET test structures or
- TCAD simulated for a different dose values [5].

In our works the model parameter sets were extracted for various SOI and SOS technologies, and different doses, and as a result SPICE model sets for CAD systems CADENCE, Mentor Graphics etc. were created.

Extraction result for H-type PD SOI MOSFETs fabricated with XFAB XI10 technology were presented at [7].

1.5. Data transfer from MOSFET structure simulation level (TCAD) to model parameter extraction level (ICCAP) with account of radiation effects

TCAD software system is not equipped with a tool assisting in transferring data to other programs. All such operations need to be programmed by the user himself.

To automate data transfer from TCAD to IC CAP we developed a number of scripts with the use of the Tcl language to be called within the TCAD Inspect environment. The scripts collect all the necessary data from among TCAD simulation results and format them according to IC CAP input file format.

Two scripts have been developed. One of the scripts addresses DC data and the others deal with CV data.

1.6. IC and VLSI simulation with radiation effects

The generated SOI/SOS MOSFET model parameter sets are used then for radiation hardness simulation with modern CAD systems. For example, Spectre and UltraSim from Cadence were used.

The developed SPICE models were successively used to simulate analog IC (see [7]) and digital VLSI characteristics with account of total dose effects. The models gave the possibility to simulate circuits and to enhance their hardness by circuit optimization.

2. Summary

The multi-level methodology for CMOS SOI/SOS IC and VLSI element parameterization with radiation effects is described.

The key point of the described methodology is thorough approach from IC manufacturing simulation to MOSFET SPICE model generation including irradiated test structures research.

The methodology includes:

1) TCAD analysis of SOI/SOS MOSFET characteristics with radiation effects before transistor real production. TCAD calibration by comparison the simulated characteristics of irradiated MOSFETs with the measured ones is used.

2) Investigation of SOI CMOS test structure behavior in radiation environment,

3) Data transfer from MOSFET structure simulation level (TCAD) to model parameter extraction level (ICCAP) with account of radiation effects,

4) SOI/SOS MOSFET SPICE model parameter generation with radiation effects using TCAD simulated or measured characteristics.

The generated model parameters are used then for SOI/SOS ICs and VLSI radiation hardness simulation with modern CAD systems.

The experience of methodology application for radiation hardened digital and analog ICs design confirmed its effectiveness for IC radiation hardness enhancement.

The results show a good correlation between predicted and measured data for wide range of functional LSI devices operating under radiation conditions.

It is important to note, that SOI MOSFET model parameters, generated according to the methodology allowed to identify and to harden the 'radiation weak' blocks in digital VLSI circuit and to enhance their hardness by circuit optimization.

3. References

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