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CHARGED BOARD EVENT ANALYSIS USING CIRCUIT SIMULATOR FOR PCB MOUNTED MOSFET

Kusnetsov V.V., Kechiev L.N.
Russia, Moscow, MIEM HSE

The model of CDM ESD impact on MOS transistors mounted on printed circuit boards is considered. The results of modeling is compared to results of ESD testing for test boards. The MOS transistor failure level decreasing is researched.

Keywords: ESD, CBE, CDM, circuit simulator, MOSFET

ESDs devices can accumulate static charge. If it then contacts massive metal parts (for example insertion head), rapidly discharge occurs from ESDs device to metal object. This event is known as Charged Device Model (CDM) [1].

CDM rating of ESDs devices depends on many factors. Mainly component package design determines CDM rating. Equivalent package capacitance determines charge amount, that can be accumulated by ESDs component. CDM ESD event modelling was considered in [2, 3]. In [4] is reported, that CDM ratings for ESDs devices, mounted on PCBs, decrease dramatically. So, if 3500 V CDM rating falls to 900 V, when component mounted on 12x12 inch PCB. ESDA White Paper [5] even introduces new ESD model — Charged board event model. The researches of this subject was started only in 2007-2008. There is no exact data for CDM ratings for specific ESDs devices and PCBs.

The purpose of this paper is to independently check results, declared in [4]. CDM impact model was developed and experimental measurements were taken for this purpose. The object of our research was International Rectifier power MOSFETs. Circuit model for CDM and CBE ESD events is proposed. Physical parameters of object is replaced by equivalent circuit components parameters in our model.

CDM ESD event equivalent circuit for component with multiple pins is shown on figure 1. This circuit can be reduced for components with three or two pins, such as diodes and transistors.

This equivalent circuit can be simulated using general purpose circuit simulators, such as PSpice. Transient analysis need to be performed for this equivalent circuit. Open-source circuit simulator Qucs was selected for performing simulation in this research. The advantage of Qucs is that it is free and open-source and allows to perform transient analysis with

picoseconds step, because not all commercials circuit simulators support picosecond transient analysis.

International Rectifier power MOSFET IRF510 was chosen as object of this research. MOSFET is basic unit of all modern semiconductor components, and results obtained for MOSFET can be extended to more complex semiconductor devices. This MOSFET has class C4 (1000 V) CDM rating.

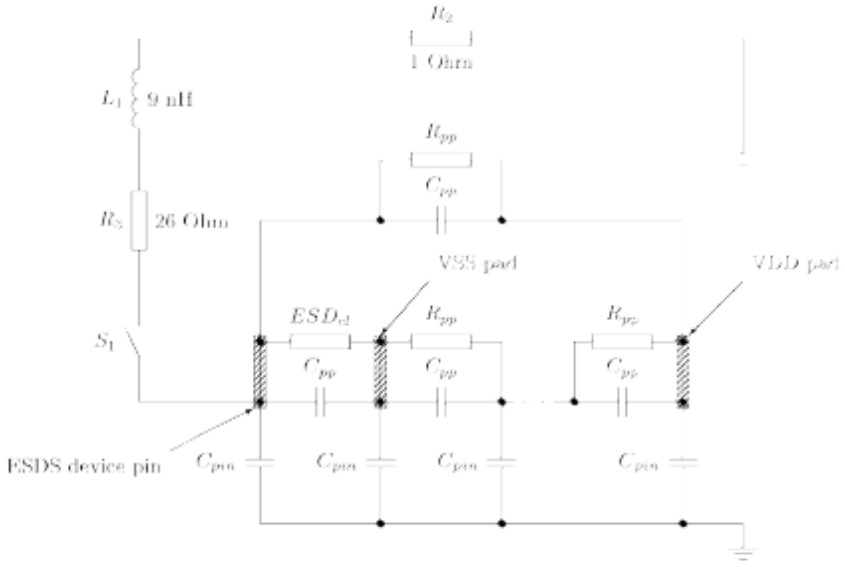

Figure 1 . The CDM ESD event equivalent circuit. R2 — current sensor resistor; R3 — arc resistance; C_{pin}=1-5pF — ESDS device pin to ground capacitance; C_{pp}=1-5pF — pin to pin capacitance; R_{pp}»1MOhnm — leakage resistance; ESD_{cl} — ESD clamp circuit.

Now having CDM event equivalent circuit, we can simulate CDM impact for IRF510 MOSFET using Qucs. IRF510 under CDM impact in Qucs shown on figure 2. Standard library model for IRF510 was used without any special adaptations. C2 on this figure is capacitance of PCB ground plane, connected to source. If there is no PCB, it can be set to few picofarads.

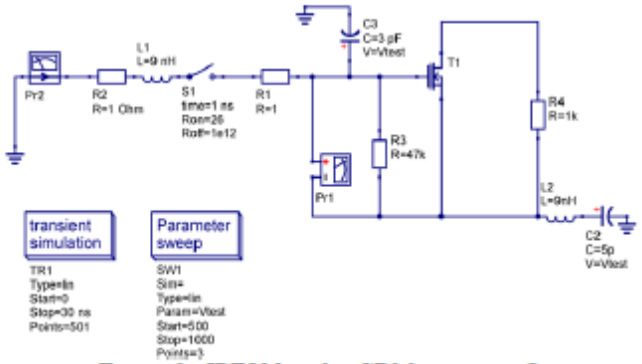

Figure 2 . IRF510 under CDM impact in Qucs.

We can perform transient analysis for this circuit and research gate-source voltage (Vgs) waveform. If Vgs voltage exceeds gate dielectric breakdown level (75 - 80 V for IRF510), MOSFET fails. Having Vgs waveform, we can determine CDM voltage level at which transistor fails. To simulate CBE event it is need to increase C2 to PCB capacitance (for example Cpcb=190 pF for test board).

Resulting transient MOSFET gate voltage waveform is shown on figure 3. Test voltage is 250V. You can see, that peak gate voltage exceeds breakdown level (75 V for IRF510). It means, than MOSFET must fail after CDM event. If test board accumulates static voltage at level 250V, and MOSFET gate then contacts to ground, CDM event occurs and MOSFET fails.

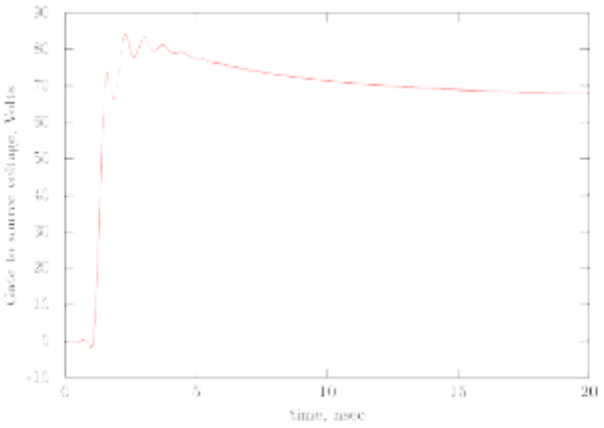

Figure 3 . CDM discharge voltage waveforms into gate of IRF510. MOSFET mounted on PCB. Test voltage 250V.

To determine CBE rating for other MOSFETs and other PCBs, it is need to do following. MOSFET spice model can be found in MOSFET datasheet and needs no adaptation. Gate dielectric breakdown voltage also can be found in datasheet. At first it is need to measure capacitance of copper polygon on PCB, connected to MOSFET source, to ground. It can be measured using general RCL-meter. Than C2 capacitance value on figure 2 need to be replaced by measured value. Transient gate voltage waveform may be obtained using transient simulation of circuit shown on figure 2. If peak gate voltage exceeds breakdown voltage at current test voltage Vtest, MOSFET fails after CDM ESD impact. You can manually increase test voltage Vtest, or use parameter sweep to determine test voltage at which peak gate voltage exceeds breakdown level.

Analysis of this model shows, that massive copper polygons on PCBs, connected to MOSFET source, store additional charge. When discharging, this charge travels to ground through MOSFET and makes additional voltage overshoots at MOSFET gate. Using this simulation method we can find CDM rating for PCB mounted MOSFET. So, CDM rating for IRF510 with test board was founded. It is 250 V. CDM rating for this transistor decreased in 4 times.

Now we can fabricate test PCB, mount IRF510 on it and perform CDM tests, using CDM ESD testing setup. Schematic of this setup is shown on figure 4. After perform test, we can compare CDM ratings, founded by modeling and by experimental testing. We should obtain same results.

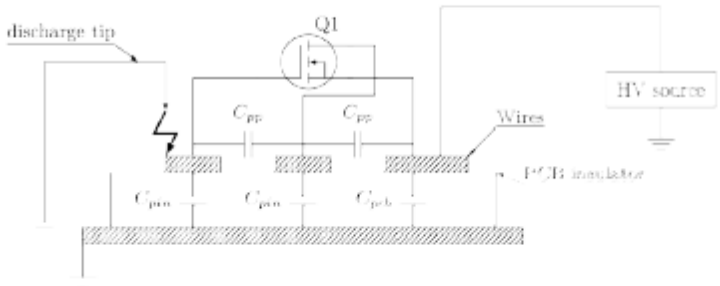

Figure 4 . MOSFET mounted on PCB under CDM impact in test setup. C_{pcb} — equivalent capacitance of ground plane connected to MOSFET source.

Failure level for IRF510 founded by experimental way was also 250 V, as for our circuit model. Difference is less than 5 % between CDM rating, founded from circuit model and CDM rating obtained experimentally. Data obtained in [4] was experimentally checked. Indeed, CDM rating for MOSFET decreases in few times. Reduction factor is more than 50 %. CDM ESD event is dangerous even for power MOSFETs, mounted on PCBs.

Having PCB capacitance value, which can be measured with general purpose equipment, and using our CDM and CBE circuit simulation method, CDM ratings for PCB mounted MOSFETs can be found.

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ELECTROSTATIC POTENTIAL METER WITH HIGH INPUT OVERSHOOTS ROBUSTNESS

Kusnetsov V.V.
Russia, Moscow, MIEM HSE

Contact electrostatic potential meter is presented. This device has high input overvoltage robustness. It can withstand 10 kV peak ESD impulse or 250 V DC voltage directly applied to its input. Measurement range can be from 5V to few kilovolts. Inverse mode vacuum tubes used in this device.

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