Thirty First Annual

# SEMICONDUCTOR THERMAL MEASUREMENT, MODELING AND MANAGEMENT SYMPOSIUM

IEEE

CPMT

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

## PROCEEDINGS 2015

San Jose, CA USA
March 15-19, 2015

NIST

National Institute of Standards and Technology




**PRINTED IN THE UNITED STATES OF AMERICA**

| | | |
|---|---|---|
| IEEE Catalog Number | CFP15SEM-USB | USB Flash Drive Edition |
| ISBN | 978-1-4799-8600-2 | |
| ISBN (USB Drive edition) | 978-1-4799-8601-9 | |
| ISSN | 1065-2221 | |


The papers from past SEMI-THERM Symposia are available from the IEEE.

**Individual papers**: www.ieee.org/services/askieee Special rates for IEEE members.

**Full printed Proceedings**: www.proceedings.com

The papers from **1987** through **2014** are available on the IEEE's **IEL/XPLORE** on-line system.

Choose to browse by conference and enter "**SEMI-THERM**" to access the full Tables of Contents, abstracts, and PDF files. Any researcher can use full-text search across the 3 million papers in the XPLORE database to access the abstracts of previous **SEMI-THERM** papers and others related to your inquiry. Subscribers may download the PDFs of any **SEMI-THERM** papers. Non-subscribers may purchase single copies at a reasonable fee. To access this resource, please visit:

**ieeexplore.ieee.org**

## SEMI-THERM Symposium Personnel

**General Chair:**
Peter Rodgers, The Petroleum Institute, UAE
prodgers@pi.ac.ae

**Program Chair:**
Rahima Mohammed, Intel Corporation
rahima.k.mohammed@intel.com

**Vice Program Chair:**
Veerendra Mulay vmulay@fb.com

**International Liaisons:**
**European Liaisons**
Clemens Lasance, Thermal Management Consultant
lasance@onsnet.nu
John Parry, Mentor Graphics john_parry@mentor.com

**Asia Liaisons**
Hsiao-Kang Ma, National Taiwan University, Taiwan
skma@ntu.edu.tw
Wataru Nakayama, ThermTech International, Japan
watnakayama@aol.com
Winston Zhang, Novark, China
winstonzhang@novark.com.cn

**Symposium Management:**
**SEMI-THERM Event Manager**
Bonnie Crystall cscomm@earthlink.net
C/S Communications, Inc.
P: +1 480 839-8988

**SEMI-THERM 31 Advisory Board**
Bernie Siegal SEMI-THERM Educational Foundation Chair
bsiegal@thermengr.net
George Meyer, Advisory Board Chair gmeyer@celsiainc.com
Jim Wilson, Finance Chair jsw@raytheon.com
Bill Maltz, Membership Chair wmaltz@ecooling.com
Tom Tarter, Technical Committee Chair
ttarter@pkgscience.com
Bruce Guenin bruce.guenin@sun.com
Clemens Lasance lasance@onsnet.nu
John Parry john_parry@mentor.com
Dave Saums dsaums@dsa-thermal.com
Ross Wilcoxon rkwilcox@rockwellcollins.com
Peter Raad praad@smu.edu
Dereje Agonafer agonafer@uta.edu
Attila Aranyosi aaranyosi@juniper.net
Sai Ankireddi sai.ankireddi@alumni.purdue.edu
Herman Chu hchu@pi-coral.com

**SEMI-THERM Exhibits Manager/ Marketing Manager**
Denise Rael drael@semi-therm.org
P: +1 408 840-2354 F: +1 408 841-7597
Marketing Assistant:
Christina Daly cdaly@thermengr.net
Webmaster: Cody Zimmer cody.zimmer@gmail.com
Graphic Design: William Schuch bill@billschuch.net
Proceedings IEEE Region 6:
Paul Wesling p.wesling@ieee.org
P: +1 408 320-1105

## SEMI-THERM 31 SELECTION AND REVIEW COMMITTEE

| | |
|---|---|
| Daniel Abishai | Intel |
| Nishi Ahuja | Intel |
| Sai Ankireddi | Soraa Inc. |
| Attila Aranyosi | Juniper Networks |
| Cath Biber | Intel |
| Patrick Bournes | Grabit Inc |
| Mihai Burzo | University of Michigan |
| Zeki Celik | LSI Corporation |
| Ming-Cheng Cheng | Clarkson University |
| Yongguo Chen | Cisco Systems |
| Herman Chu | Pi-Coral |
| Eric Dede | Toyota |
| Valerie Eveloy | The Petroleum Institute |
| Pablo Hildigo | Georgia Tech |
| Hussam Kabbani | nVidia |
| Clemens Lasance | SomelikeitCool |
| Wendy Luiten | Philips Research |
| Bonnie Mack | Magma |
| Atila Mertol | LSI Corporation |
| Genevieve Martin | Philips |
| Wataru Nakayama | ThermTech International |
| Susheela Narasimhan | Juniper Networks |
| Nader Nikfar | Qualcomm |
| Jim Petroski | Design by Analysis |
| John Parry | Mentor Graphics |
| Andras Poppe | Mentor Graphics MAD MicReD |
| Adriana Rangel | Cisco |
| Marta Rencz | Mentor Graphics, BME |
| Mauricio Salinas | Raytheon |
| Dave Saums | DS&A LLC |
| Dirk Schweitzer | Infineon |
| Ross Wilcoxon | Rockwell Collins |
| Lei Shao | University of Michigan |
| Heinz Pape | Infineon |
| Guy Wagner | Electronics Cooling Solutions |
| Kazuaki Yazawa | Purdue University |
| Winston Zhang | Novark |

## THERMI Award Winner 2015

Each year, SEMI-THERM honors a person as a Signifficant Contributor to the ffield of thermal man-agement. The THERMI award is intended to recognize a recipient's history of contributions to cru-cial thermal issues eflecting the perfor-mance of electronic devices and systems. The voting body of past THERMI winners and current General Chair Peter Rodgers are pleased to present the 2015 THERMI award to:

**Christian Belady**
General Manager, Data Center Services
Microsoft Global Foundation Services

Christian Belady is the general manager of Data Center Services for Microsoft's Global Foundation Services (GFS) group. He is responsible for driving the strategy and delivery of server and facility development worldwide, including research, engineering, construction, and operations for Microsoft's data center portfolio. These data centers provide the founda-tional cloud infrastructure for over 200 Microsoft online and cloud services for consumers and businesses worldwide.
Prior to joining Microsoft, Christian was a Distinguished Technologist for HP where he was re-sponsible for driving the technology direction of HP's server products and their environments, as well as industry data center initiatives.
In 2010, SearchData named Christian as one of "5 People who changed the data center" industry and helped drive inno-vative thinking and quantitative benchmarking in the field. With over 100 US patents and many international patents, Christian is an ASME and IMAPS Fellow and a founding member of ASHRAE's TC9.9, which is responsible for developing data center guidelines.
Christian holds engineering degrees from Cornell University (BS) and Rensselaer Polytechnic In-stitute (MS) and a busi-ness degree from the University of Texas at Dallas (MA) where he was honored with the 2010 Distinguished Alumni Award.

# The Harvey Rosten Award for Excellence, 2014

Harvey Rosten Award winners are Jesse Galloway, Cameron Nelson and Phillip Fosnot


From left to right; Jesse Galloway, Cameron Nelson and Phillip Fosnot

Cameron Nelson received a Bachelor of Science in Mechanical Engineer from Arizona State University. He joined Amkor Technology in 2010 and now leads thermal simulation characterization as a Senior Thermal Engineer. Phillip Fosnot also received a Bachelor of Science in Mechanical Engineering from Arizona State University. He joined Amkor in 2012 and now supports simulation and experimental testing of electronic packages. Jesse Galloway has over 25 years in the electronic packaging industry.  He manages the Thermal and Mechanical Characterization team at Amkor Technology in Tempe, Arizona.

Their paper from SEMI-THERM 2014, **Extracting TIM Properties with Localized Transient Pulses**, is included with this Proceedings, for your awareness.

## SEMI-THERM TECHNICAL SHORT COURSES

Highly informative short courses were offered Sunday March 15 - Monday March 16, 2014. These outstanding technical courses are focused on the thermal sciences and are presented by leaders in the thermal field.

**Short Course 1: Crash Course on Packaging Technologies and Thermal Design of ICs**


**Li Li, PhD, Distinguished Engineer, Cisco Systems**
**Herman Chu, Principal Engineer, Cisco Systems**

The course covers:

- Overview of various types of IC packages and their targeted application(s), advantages and limitations.
- Describe the construction, materials and assembly processes associated with IC packages.
- Understand the influence of various package design parameters on the thermal, electrical and thermo-mechanical reliability performance of the package.
- Discussion of typical failure modes associated with IC packages and identify the common stress drivers.
- Future IC packaging trends.

**Short Course 2: Use of Flow Network Modeling ( FNM) for Improving Productivity of Design of Electronic Cooling Systems**


**Kanchan M. Kelkar, Ph.D., Innovative Research, Inc.**
**Sukhvinder Kang, Ph.D., Aavid Thermalloy**

As the complexity and power density of electronics systems increase, there is an ever-increasing demand for methods and tools to improve the quality of the product and the productivity of the designers. The Flow Network Modeling (FNM) technique achieves this by focusing on the analysis of the interaction among the cooling components to determine system-level performance in a rapid and accurate manner. The short course will discuss the details of the FNM technique and illustrate its use in the thermal design process of air- and liquid-cooling systems.

The specific topics to be covered in the course are as follows:

- Overview of the FNM technique • Overall design process and role of Flow Network Modeling
- Complementary use with CFD • Theoretical Basis of FNM
- Construction of the flow network of a cooling system
- Overall flow and thermal characteristics of cooling components using loss factors from handbooks and measured data
- Characteristics of commonly encountered components such as ducts/tubes, orifices, screens, heat sinks and cold plates, heat exchangers, fans and pumps
- Overall solution method for network analysis and results obtained
- Practical Use of Flow Network Modeling
- Use of hand calculations for analysis of an air cooling system
- Use of spreadsheets for analysis of air and liquid-cooling systems
- Generalized flow network analysis of practical systems using the commercial software MacroFlow

## Flexible Data Center Design

Building a global network of efficient, large-scale data centers requires flexible designs to accommodate local conditions and constraints, while accommodating rapidly changing IT hardware and software requirements. This presentation will discuss some of the approaches we've taken and how Google continues to improve data center efficiency.

**Christopher G. Malone, PhD**
**Principal Engineer, Google, Inc.**

Chris leads Google's Data Center Research and Development team, which is responsible for developing Google's next-generation data centers and IT hardware with a focus on efficiency, sustainability, and flexibility. Chris has authored numerous refereed technical papers, and has been granted over 100 US and international patents. He is involved with several industry groups and government agency initiatives focused on improving IT efficiency. Prior to joining Google, Chris was a senior technologist at Hewlett-Packard responsible for enterprise server thermal technology strategy.

Chris received his MS and PhD in Mechanical Engineering from the Massachusetts Institute of Technology.

THERMAL INNOVATIONS THAT MAKE THE WORLD'S TECHNOLOGY COOL...

# ST31 Embedded Tutorial

## Thermal Challenges of 2.5D and 3D Integration

Dr. Herman Oprins, IMEC

This embedded tutorial will present an overview of the thermal challenges of 2.5D (interposer) and 3D integration. The tutorial compares the thermal performance and thermal die-to-die coupling of single chip, 3D and 2.5D package configurations. The thermal impact of the inter die thermal resistance as well as the design and technological options of how to reduce this resistance will be discussed. The tutorial describes thermal test vehicles for uniform, hot spot and programmable power dissipation to emulate target applications. A short overview of modeling techniques and experimental validation approaches is included. Finally, the experimental and modeling analysis will be shown for the case study of a packaged memory-on-logic stack, which is one of the most likely applications of 3D integration.

**About the Speaker**

**Dr. Herman Oprins** is a senior research engineer at IMEC in Leuven, Belgium, where he is involved in the thermal experimental characterization, thermal modeling and thermal management of 3D system integration, electronic chip packages, GaN power transistors, photovoltaic modules and microfluidics. Dr. Oprins began his career at IMEC working on the development and modeling of an electrowetting assisted cooling technique. In that period he also worked on modeling and experimental projects in the field of thermal management of electronic packages. Oprins has authored and co-authored over 60 journal and conference papers and holds 2 patents. He hold M.Sc. and Ph.D. degrees in Mechanical Engineering from the K.U. Leuven, Belgium.

# Luncheon Talk: "Application and Characterization of Soft Tissue Ablation by Radio Frequency"

**Luncheon Abstract:** "Radiofrequency (RF) ablation of soft tissue in biomedical application, to wit, atrial fibrillation has been well established. The ablation process thermally destroys tiny areas in the heart that are firing off abnormal electrical impulses causing atrial fibrillation. However use of RF ablation for renal artery denervation is a very recent technique and has revolutionized the treatment of refractory, drug-resistant hypertension. The renal denervation technique has also shown early promise in end stage renal disease (ESRD), and congestive heart failure (CHF) patients.

Design space involves key variables such as electrode shape and dimension, procedural contact impedance, apposition, residence time, and need for coolant circulation to minimize collateral tissue damage. All of these variables can be influenced by real-time detection of the thermal front progressing into the tissue. Hence real-time tissue damage sensing either through a parametric, predictive algorithm or by biochemical marker detection is of paramount importance. Few options will be discussed as an introduction to this topic."

## Bio: SYED FAIYAZ AHMED HOSSAINY

Syed Hossainy, PhD is a senior research fellow at Abbott Vascular. Syed has recently been the head of Abbott Vascular's innovation incubator group (operating budget ~ $4.5 MM /yr) with a Vision of "Targeted innovation optimizing short-term and long-term business growth options".
The group has delivered 10 successful proof-of-feasibility projects completed and readied for advanced development between 2007-2013. Five of these became late-stage development projects. Successful development projects include Bioabsorbable Vascular Scaffold for peripheral vasculature, currently being tested clinically. Formulated and led technical strategy to advance Drug-eluting stent (DES) and Bioabsorbable Vascular Scaffold (BVS) clinical performance attributes. Syed's technical contributions include:

- **Local Drug delivery**: Developed controlled release technology for combination drug-device application, specifically drug eluting stent (DES) and Bioabsorbable implant technology;
- **Mathematical model:** Developed predictive computational tools for DES application and local Pharmacokinetics; and BVS structure property and mechanical coupling with vessel
- **IP strategy**: Created IP strategy for the entire business unit by partnering with legal.
- **Patent awards:** Over 280 issued patents, Over 380 patents pending (listed in USPTO) in the area of cardiovascular implants, drug delivery, and Biomaterials application.

# TABLE OF CONTENTS

## SEMICONDUCTOR THERMAL MEASUREMENT AND MANAGEMENT SYMPOSIUM

## Session 4: Modeling and Characterization
Chair: Marta Rencz
Co-Chair: Jacob Supowit



## Session 5: Data Center II
Chair: Veerendra Mulay
Co-Chair: Alistair Waddell

## Session 9: Measurements and Characterization II
Chair: Peter Rodgers
Co-Chair: Jacob Supowit



## Session 10: Computational Fluid Dynamics Analysis Modeling
Chair: William Maltz
Co-Chair: Tianyi Gao



## Session 11: Enhanced Heat Transfer
Chair: Guy Wagner
Co-Chair: John Maddox

## Session 12: Quality and Reliability

Chair: Rahima Mohammed

Co-Chair: Husam Alissa



---

# Electro-Thermal Modeling of Trench-Isolated SiGe HBTs Using TCAD

K. O. Petrosyants [1,2], R. A. Torgovnikov [2]
[1] National Research University Higher School of Economics
(Moscow Institute of Electronics and Mathematics), Moscow, Russia, kpetrosyants@hse.ru
[2] Institute for Design Problems in Microelectronics, Russian Academy of Sciences

**Abstract**

The modern SiGe HBT structure with shallow and deep trench isolation (STI and DTI) is analyzed from electro-thermal standpoint using TCAD system. The electrical parameters β, $f_T$, $f_{\max}$, maximal temperature $T_{\max}$, and thermal resistance $R_{TH}$ are under consideration. TCAD simulation confirms the fact that the presence of STI and DTI in SiGe HBT structures gains the self-heating effect in comparison with traditional Si BJT structures, where DTI is not used. It is shown that for high power regimes ($I_C$ = 0.5–3 mA; $V_{CE}$ = 4–5 V) the set of electrical parameters β, $f_T$, $f_{\max}$ significantly degrade, temperature $T_{\max}$ can reach the critical values about 500 K, and the thermal resistance $R_{TH}$ increases thrice in HBT structure with STI and DTI. These results agree with published experimental data.

**Keywords**

Silicon-Germanium HBT, transistor structure, trench isolation, high power/high frequency electrical parameters, electro-thermal design, temperature distribution, maximal operation temperature, thermal resistance

## 1. Introduction

The Silicon-Germanium heterojunction bipolar transistors (SiGe HBT) are good choice for modern high power and high frequency ICs. However, it is well known that the device temperature increases significantly in high power and high speed applications to cause degradation of the device characteristics. For SiGe HBTs this problem is more critical than for traditional Si BJTs. The thermal conductivity of the SiGe base alloy ($\lambda_{SiGe}$ = 14 W/m·K for $T$ = 300 K) is significantly lower than that of the Si ($\lambda_{Si}$ = 150 W/m·K). So the self-heating effects are further enhanced in the SiGe HBTs due to the increase of the thermal resistance and hot-spot formation. Moreover, in the SiGe HBT structure Silicon dioxide ($SiO_2$) shallow and deep trench isolation is used to improve gain and high frequency parameters and press the leakage current. The thermal conductivity of the Silicon dioxide ($\lambda_{SiO2}$ = 1.38 W/m·K) is 100 times lower than that of Silicon and the oxide-based trenches behave as a heat insulators. For this reason, the heat dissipation from the SiGe HBT active region becomes more critical. So an accurate determination of the temperature distribution in 2D–3D device structure is required to specify the maximal temperature $T_{\max}$ and thermal resistance $R_{TH}$ to guarantee the electro-thermal stability and operate reliability.

Several models using 2D/3D TCAD simulation have been investigated to take into account self-heating effects in SiGe HBTs. In [1] the 2D HBT structure without trench isolation has been analyzed taking into account only SiGe base alloy influence on electro-thermal behavior. In [2] 3D thermal TCAD simulations have been carried out to obtain transient variations of the junction temperature in SiGe HBT. In paper [3] intra device thermal coupling in multi-finger HBT structures has been studied.

However, all these works did not consider the combined influence of the SiGe base alloy and the shallow and deep trench $SiO_2$ isolations on the SiGe HBT electro-thermal characteristics. Therefore, the published results did not represent completely the self-heating problems in modern trench-isolated SiGe HBT structures.

In this work, we try to solve the problem in more details.

## 2. Electro-Thermal Model of SiGe HBT Structure

The modern self-aligned SiGe HBT structure with emitter size 0.2*1.0 μm², selective implanted collector, shallow and deep trench isolation, providing the following electrical parameters: $\beta_{\max}$ = 413, $f_T$ = 93 GHz, $f_{\max}$ = 160 GHz, $BV_{ceo}$ = 5.7 V [4] was taken under consideration.

The thermo-dynamic model in Synopsys Sentaurus software tool was chosen for SiGe HBT structure electro-thermal simulation. This model consists of four basic 2D equations: two equations for electrons (n) and holes (p) transport (Eq. (1) and (2)), Poisson equation for electro-static potential φ distribution (Eq. (3)) and heat transfer equation, taking into account transistor structure self-heating caused by power density H (Eq. (4)):

$$j_n = -q\mu_n n\left(\nabla\phi_n + P_n\nabla T\right), \tag{1}$$

$$j_p = -q\mu_p p\left(\nabla\phi_p + P_p\nabla T\right), \tag{2}$$

$$\nabla^2\varphi = \frac{q}{\varepsilon}\left(p + N_D - n - N_A\right), \tag{3}$$

$$\nabla(\lambda\nabla T) - H(j_n, j_p, \varphi, T) = \rho C\frac{\partial T}{\partial t}, \tag{4}$$

where: $\nabla = \frac{\partial}{\partial x}\bar{i} + \frac{\partial}{\partial y}\bar{j}$ ; λ – specific heat conductivity (W/m·K), ρ – density of material (kg/m³), $C$ – specific thermal capacitance (J/kg·K), ε – dielectric constant of the material (F/m); $T(x,y)$, $\varphi(x,y)$ – temperature and electrostatic potential distributions; $j_n(x,y)$, $j_p(x,y)$, $P_n(x,y)$, $P_p(x,y)$, $\phi_n(x,y)$, $\phi_p(x,y)$ – current densities, absolute thermoelectric powers, quasi-Fermi potentials for electrons and holes, respectively; $N_D(x,y)$, $N_A(x,y)$ – donor and acceptor doping concentrations in transistor structure.

All effects inherent in modern SiGe HBT structures are specially included into the equations of the basic model (1)–(4) [5]. The majority of the self-generated heat is dissipated downward towards the substrate. This heat flow is described by the basic model. Some amount of the heat is dissipated upward as well, mostly through the metal wiring for interconnect. Hence in this model, an external element $R_{therm}$ is introduced as a fitting parameter to account for the upward dissipation. For our HBT structures $R_{therm}$ = 65 000 K/W was assumed [6].

## 3. Simulation Results with Account for Self-Heating

The "step-by-step" modeling strategy is used to investigate the self-heating effects in trench-isolated SiGe HBT structures. At first, the influence of the SiGe base alloy is separately analyzed. Then only the STI is added, and the new device structure is analyzed. Finally, the DTI is added and the real SiGe HBT structure with both STI and DTI is considered taking into account all the factors that have an influence on self-heating.

### 3.1. SiGe base alloy influence

SiGe base alloy in HBT structure behaves as an internal barrier for the heat flow from collector to emitter region due to the significantly lower thermal conductivity of SiGe than that of Si (14 versus 150 W/m·K at $T$ = 300 K). This effect is important for intra-active device region E–B–C. To separate the contribution of this effect to the total device heating we have compared active SiGe HBT structure (without trenches) with identical Si BJT structure. The 2D temperature profiles for both transistor active regions are shown in Fig. 1 (for the same power dissipation). The peak temperature $T_{\max}$ in collector region of SiGe HBT structure is 409 K (see Fig. 1,*b*) that is 18 K higher than for Si BJT structure (see Fig. 1,*a*). This difference in 2D temperature distributions is caused by differences in thermal conductivities of Si and SiGe.

It is interesting to analyze the temperature distribution along the depth of active transistor structure (see Fig. 2). The temperature in Si BJT structure is distributed more uniformly than in SiGe HBT structure. It is clear that SiGe base alloy with low thermal conductivity is working as a barrier for heat dissipation in the direction of the emitter. This has two negative consequences: the high value of peak temperature $T_{\max}$ and abrupt drop in temperature distribution. Therefore, the self-heating effects in the internal active region of SiGe HBT are more critical than in identical Si BJT. As observed in Fig. 3, where transistor output characteristics are presented, the Early voltage $V_A$ degradation in the SiGe HBT (from 34 V to 11 V after self-heating) is more apparent in comparison with Si BJT (from 13 V to 8 V).

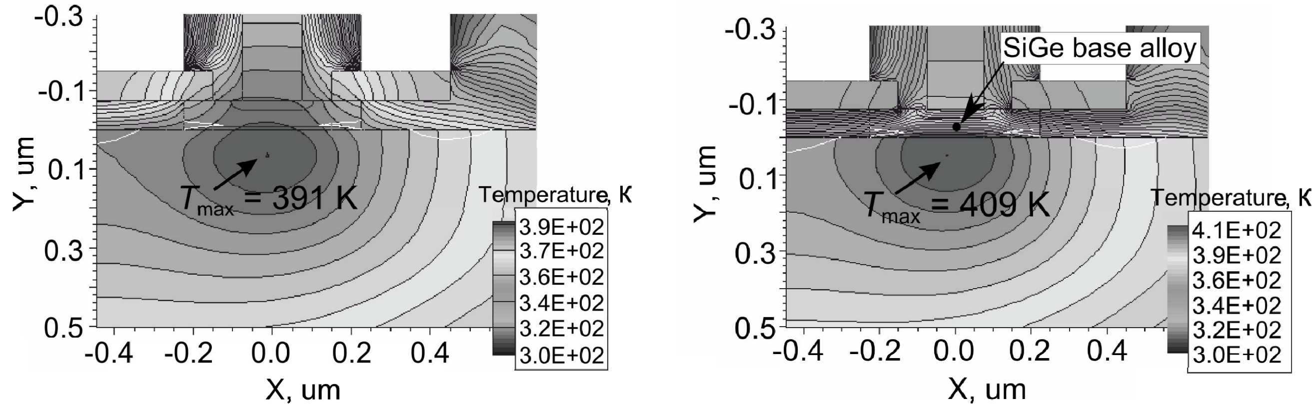


**Fig. 1:** 2D temperature distribution in Si BJT (a) and SiGe HBT (b) structures for $P_{total}$ = 0.01 W

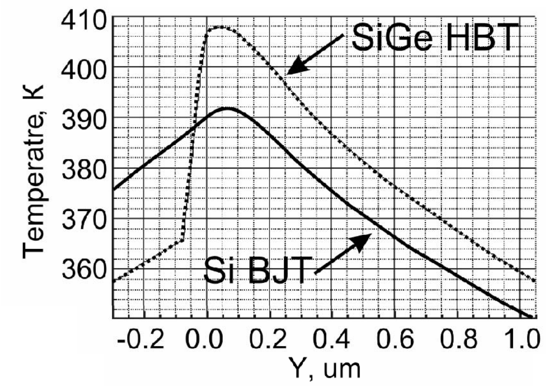


**Fig. 2:** Temperature distributions along the transistor internal active region cross-sections ($X$ = 0.0 µm) for Si BJT and SiGe HBT structures in Fig. 1

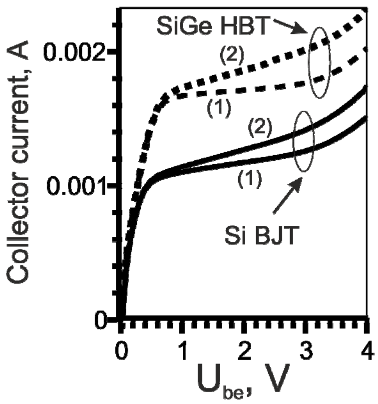


**Fig. 3:** I-V output characteristics for Si BJT (solid lines) and SiGe HBT (dotted lines) simulated without (1) and with (2) account for self-heating

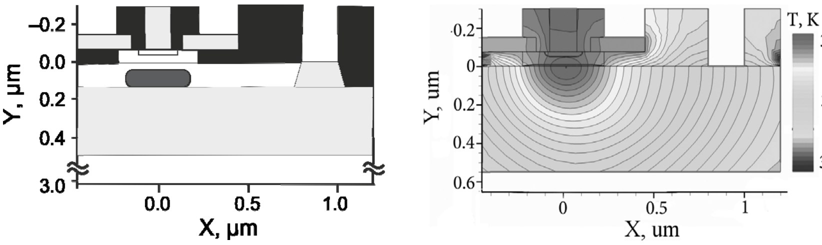


**Fig. 4:** Hypothetic SiGe HBT structure without oxide trench isolation (a), its temperature distribution at $I_C = 2$ mA, $V_{CE} = 1.5$ V, $T_{\max} = 323$ K (b)

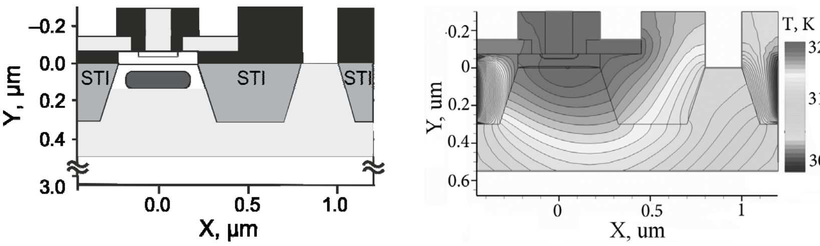


**Fig. 5:** SiGe HBT structure with shallow trench isolation (a), its temperature distribution at $I_C = 2$ mA, $V_{CE} = 1.5$ V, $T_{\max} = 326$ K (b)

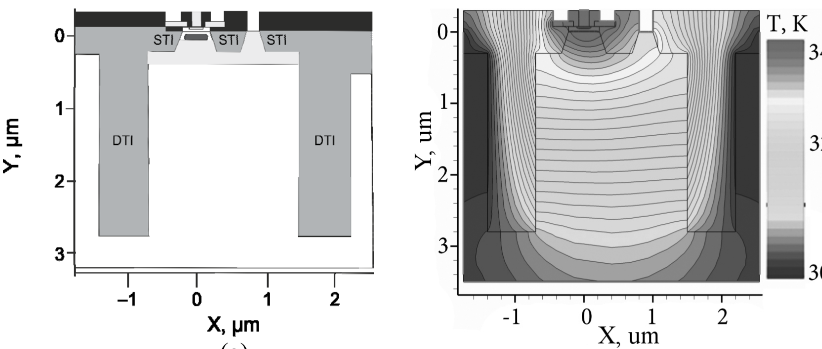


**Fig. 6:** SiGe HBT structure with both shallow and deep trench isolation (a), its temperature distribution at $I_C = 2$ mA, $V_{CE} = 1.5$ V, $T_{\max} = 340$ K (b)

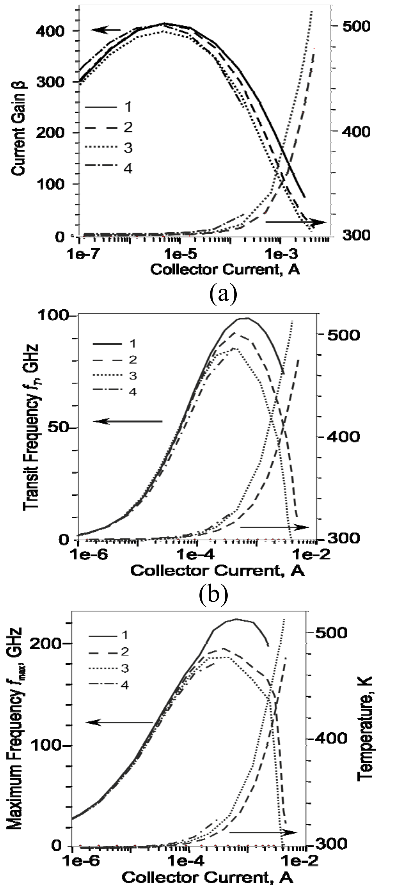


**Fig. 7:** Current gain β (a), transit frequency $f_T$ (b), maximum frequency $f_{\max}$ (c) at $V_{CE} = 5$ V: 1 – for all the structures without account for self-heating, 2 – structure without trench isolation, 3 – structure with shallow trench isolation, 4 – structure with both shallow and deep trench isolation

### 3.2. Oxide-based trenches influence

To understand the contribution of either of STI and DTI to total device heating, the hierarchy of three transistor structures was analyzed: without trench isolation (Fig. 4,*a*); only with STI (Fig. 5,*a*) and with both STI and DTI (Fig. 6,*a*).

The corresponding set of transistor characteristics for current gain β, frequencies $f_T$, $f_{\max}$, and junction temperature $T_j$ vs. collector current $I_C$ taking into account self-heating effect was simulated using the basic model (1)–(4) (see Fig. 7). The collector currents $I_C = 0.5$–$2$ mA are interesting because these currents make available high values of operating frequencies $f_T$, $f_{\max}$ and acceptable values for current gain β. Two regimes for $V_{CE}$ are considered: low-voltage $V_{CE} = 1.5$ V and high-voltage $V_{CE} = 5$ V.

The simulated 2D temperature distributions for three types of HBT structures are presented in Fig. 4,*b* (without trench isolation), Fig. 5,*b* (with STI only) and Fig. 6,*b* (with STI and DTI).

The simulation results are summarized in Tables 1, 2 for different levels of power dissipation ($P_{total} = I_C*V_{CE} + I_B*V_{BE}$). It is seen from Table 1 for low power regime ($I_C = 1$–$2$ mA; $V_{CE} = 1.5$ V) that self-heating effects can be neglected. However, in Table 2 for high power regime ($I_C = 1$–$2$ mA; $V_{CE} = 5$ V) the set of electrical parameters β, $f_T$, $f_{\max}$ significantly degrade, and temperature $T_{\max}$ reaches the critical values about 500 K.

STI influence on HBT self-heating. For low and high-power regimes, this factor is neglectable. The temperature difference 20–30 K between values in the 1-st and the 2-nd columns of Table 2 is caused mainly by SiGe base alloy influence (see Fig. 1), but not by STI. As mentioned in [6], the STI influence on HBT RF characteristics is not significant and is about 8% in experiment.

DTI influence on HBT self-heating. The internal space between deep oxide-based trenches in SiGe HBT structure (Fig. 6,*a*) behaves as a narrow-pinched channel for heat dissipation because $SiO_2$ material is a good thermal isolator with low thermal conductivity ($\lambda_{SiO2} = 1.38$ W/m·K at $T = 300$ K). Therefore, DTIs are the main factor that stimulates the self-heating effects and causes the electrical and thermal HBT parameters degradation. It is seen from Fig. 7 that the 10–20 % degradation of electrical parameters $\beta$, $f_T$, $f_{\max}$ is observed. The peak temperature increase $\Delta T_{\max}$ for low-power regime is 8–14 K (see Table 1) and for high-power regime 33 K and more (for $P_{total}$ more than 0.01 W temperature $T_{\max}$ can reach the critical values about 500 K) (see Table 2).

| Transistor structure | Without trench isolation (Fig. 4) | STI (Fig. 5) | STI + DTI (Fig. 6) |
|---|---|---|---|
| Maximum temperature, K, at $I_C$ = 1 mA/ 2 mA | 312 / 323 | 315 / 326 | 323 / 340 |

**Table 1:** Peak temperature $T_{\max}$ in different HBT structures for low-power regime at $V_{CE} = 1.5$ V

| Transistor structure | Without trench isolation (Fig. 4) | STI (Fig. 5) | STI + DTI (Fig. 6) |
|---|---|---|---|
| Maximum temperature, K, at $I_C$ = 1 mA/ 2 mA | 347/388 | 367/424 | 400/ $> T_{crit}$ |

**Table 2:** Peak temperature $T_{\max}$ in different HBT structures for high-power regime at $V_{CE} = 5$ V

| Transistor structure | Without trench isolation (Fig. 4) | STI (Fig. 5) | STI + DTI (Fig. 6) |
|---|---|---|---|
| Thermal resistance, $R_{TH}$, K/W | $12 \cdot 10^3$ | $20.5 \cdot 10^3$ | $30 \cdot 10^3$ |

**Table 3:** HBT structures thermal resistance

### 3.3. Thermal resistance $R_{TH}$

Thermal modeling is necessary for a precise prediction of $R_{TH}$ that is a crucial parameter for optimization of device structure. The reduction of $R_{TH}$ is actually as effective as the reduction of power dissipation for a single device.

Using simulated results, the thermal resistance $R_{TH}$ was extracted for three types of HBT structures (see Table 3). It is seen that for the structure with STI only (Fig. 5,*a*), in comparison with the hypothetic structure without trench isolation (Fig. 4,*a*), the value of $R_{TH}$ increases twice. The combination of DTI and STI additionally increases $R_{TH}$ 1.5 times.

These results agree with published experimental data [6, 7].

## 4. Conclusions

The methodology of TCAD electro-thermal modeling of trench-isolated SiGe HBTs is proposed. Three most important elements of HBT structure causing self-heating were chosen: SiGe base alloy, STI and DTI. Their contribution to total device heating was separately analyzed in details. It was shown that in modern SiGe HBT structures: 1) the SiGe base alloy forms the internal barrier for heat dissipation through the active HBT structure; and 2) the oxide-based trench isolation is the main factor that enhances the self-heating effect in comparison with traditional Si BJT structures. The influence of STI and DTI on thermal resistance $R_{TH}$ was investigated. It was shown that presence of STI in SiGe HBT structure increases the value of $R_{TH}$ twice, and the combination of STI and DTI – thrice.

As the requirements to the parameters of modern high-speed and high-power SiGe HBTs continue to strengthen, the proposed TCAD modeling methodology is an effective means for HBT structures improvement in thermal and electrical performances to provide thermal stability and operation reliability.

## References


1. Mukherjee C., Maiti C. K., “Simulation and Modeling of Self-Heating Effects in Heterojunction Bipolar Transistors,” Journal of Basic and Applied Physics, vol. 3, iss. 1, pp. 16-25, 2014.
2. Sahoo A. K. et al., “A scalable electrothermal model for transient self-heating effects in trench-isolated SiGe HBTs,” IEEE Trans. on Electron Devices, vol. 59, no. 10, pp. 2619-2625, 2012.
3. Weiß M. et al., “Characterization of intra device mutual thermal coupling in multi finger SiGe: C HBTs,” Proc. IEEE International Conf. of Electron Devices and Solid-State Circuits (EDSSC), pp. 1-2, 2013.
4. P. Chevalier, C. Fellous, Z. Rubaldo et al., “230 GHz Self-Aligned SiGeC HBT for Optical and Millimeter-Wave Applications,” IEEE J. of Solid-State Circuits, vol. 40, no. 10, 2005, pp. 2025–2034, 2005.
5. Synopsys TCAD Sentaurus, ver. J-2014.09, Online: www.synopsys.com.
6. Jae-Sung Rieh, D. Greenberg, Qizhi Liu; et al., “Structure optimization of trench-isolated SiGe HBTs for simultaneous improvements in thermal and electrical performances,” IEEE Trans. on Electron Devices, vol. 52, no. 12, pp. 2744 – 2752, 2005.
7. Yang, LF et al., “Si/SiGe heterostructure parameters for device simulations,” Semiconductor Science and Technology, vol. 19, no. 10, pp. 1174-1182, 2004.



This work was supported by the National Research University–Higher School of Economics’ Academic Fund Program in 2015, grant No. 15-01-0165, and by Russian Foundation for Basic Research, grant No.14-29-09145.