2019 International Siberian Conference on Control and Communications (SIBCON)

Laboratory Bench for Predicting the Reliability of Wireless Devices Based on the NI MyRIO Platform

Valery Zhadnov
School of Electronic Engineering
National Research University
"Higher School of Economics"
Moscow, Russia
vzhadnov@hse.ru

Pavel Korolev
School of Electronic Engineering
National Research University
"Higher School of Economics"
Moscow, Russia
pskorolev@hse.ru

Anton Sosnin
School of Electronic Engineering
National Research University
"Higher School of Economics"
Moscow, Russia
aisosnin@edu.hse.ru

Kirill Sedov
School of Electronic Engineering
National Research University
"Higher School of Economics"
Moscow, Russia
kdsedov@edu.hse.ru

***Abstract* — The report discusses the use of National Instruments tools for dependability prediction of electronic devices by simulation modeling. The description of the laboratory bench allowing to develop formal models based on reliability block diagrams, to carry out simulation experiment and to process statistical modeling results, is given as well as an example of this bench usage for reliability prediction of power supply of the lightweight spacecraft.**

***Keywords* — wireless device, faultlessness, redundancy, MyRIO, lightweight spacecraft, simulation modeling.**

I. Introduction

One of the main means of ensuring Radio Technical Devices (RTD) dependability is redundancy, which is used to ensure the RTD reliability as a whole, i.e. to maintain their performance in case of failure of one or several insufficiently reliable Incoming Components (IC).

Enterprises developing and manufacturing RTD for various equipment, especially those operating under severe conditions, face problems of ensuring dependability, in particular, reliability [1]. This is confirmed by both failures at the stages of RTD acceptance checkout and their failures during operation.

A promising direction in the field of dependability, as well as the characteristics assessment of dependability indicators is simulation modeling [2].

There are professional subsystems (software systems) for reliability characteristics calculation, for example, ASONIKA-K-SI [3, 4]. However, such subsystems have a significant drawback, since use computing power of the computer, which during simulation can cause considerable time costs with a large number of IC.

This drawback can be eliminated due to the use of Field-Programmable Gate Array (FPGA) technology using a shift register algorithm with linear feedback [5]. Therefore, the development of a laboratory bench (software and hardware complex) for predicting the quantitative characteristics of RTD faultlessness (such as Reliability Function - *R* and Mean Operating Time to Failure - T_0) becomes relevant, what can be accomplished using technologies from National Instruments, namely LabView (Laboratory Virtual Instrumentation Engineering Workbench) software complex and NI MyRIO multi-functional reconfigurable platform. Thus, it is planned to achieve an increase in the efficiency of calculating the faultlessness characteristics of complex radio technical devices.

II. Laboratory bench structure

The laboratory bench for predicting the dependability of RTD, in particular, the reliability characteristics by RTD, includes three main components: a personal computer, a multifunctional reconfigurable platform NI MyRIO and an engineering laboratory workstation NI ELVIS (see Fig. 1).

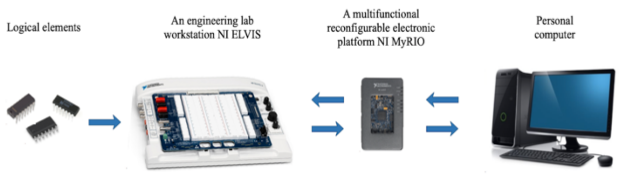

Fig. 1. The composition of the laboratory bench for reliability prediction of RTD

A. The role of the personal computer

The computing process is controlled using a personal computer with a special software package installed that is compatible with the NI MyRIO multi-functional reconfigurable platform [6]. This requirement is met by LabVIEW - graphical application development environment developed by National Instruments. With this software, the NI MyRIO platform could be programmed as well as the statistical processing of the obtained data could be carried out according to the results of the simulation modeling.

B. The role of NI MyRIO platform

The multifunctional reconfigurable platform NI MyRIO is an intermediate between a personal computer and an engineering laboratory workstation NI ELVIS. However, it plays a key role in the entire bench (see Fig. 1), since it receives information through the input ports, forms the type of signals and delivers the necessary effects through the output ports.

The National Instruments hardware-software approach, commonly referred to as reconfigurable input/output architecture, is based on four main components: a processor, FPGA, input/output, and graphics software [7]. Figure 2 represents NI LabView RIO architecture.

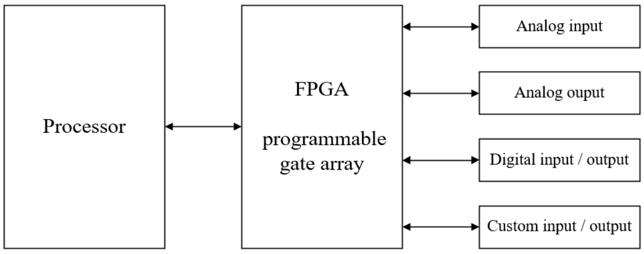

Fig. 2. The NI LabView RIO architecture

In the aggregate, these components provide the ability to quickly create specialized hardware circuits with high-performance input/output and flexibility in system management.

FPGA is a logical element (“AND”, “OR”, etc.) on a single chip, and the logic of work is set by the user.

In contrast to the microcontroller, which is used more to perform chains of commands, their cyclic repetition, switching from one chain to another, etc., FPGA, in turn, is mainly used to perform simple logical operations and, crucially, a large number of them at the same time, using different clock frequencies [8].

FPGA has memory boxes, configurable logic boxes (CLBs), multiplication boxes and digital signal processors (DSPs), input/output boxes, programmable interconnects (see Fig. 3).

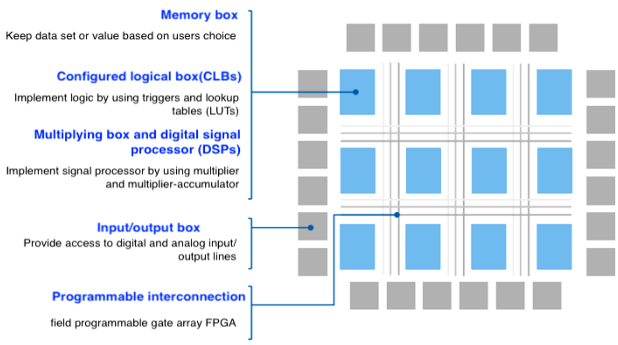

Fig. 3. FPGA technology

The circuit design is performed in a hardware description language, which is then synthesized into bitstreams before being written to the FPGA core. Compared to other logical devices, FPGA has a very high logical density. This means that one chip contains from ten thousand to eight million gates. Therefore, complex logic circuits are implemented using FPGA.

The user himself programs the required circuit on FPGA devices. The main advantage is the ability to reprogram the device. Therefore, in most cases, such a technical solution is the most preferable at the design stage, as there may be permanent unforeseen changes in the scheme.

C. The role of the NI ELVIS Engineering Laboratory Station

The NI ELVIS engineering laboratory workstation serves as a breadboard for assembling an electrical circuit diagram on logic elements - an imitation of a “Reliability Block Diagram” (RBD), as well as for displaying waveforms of signals, measuring voltages at control points, and ensuring stable power supply.

III. SIMULATION MODELING PROCESS

The simulation process includes 3 stages (see Fig. 4).

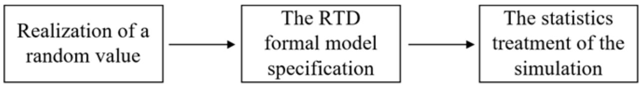

Fig. 4. Simulation modeling process

The first stage is the acquisition of realizations of random variables, the second is the imitational experiments on the formal model of RTD, and the third is the statistical processing of the simulation results.

The calculated estimate of the reliability characteristics quantitative values redundant by RTD with high accuracy is possible due to the simulation modeling method (Monte-Carlo Method) [9].

This is achieved by an adequate description of their structure and, if necessary, reconfiguration algorithms in formal model.

The essence of this method is as follows: for the basic random variable x, distributed according to a uniform law on the interval $[a; b]$ generates a set of random values of N, and then, based on it, the required values u_i.

The accuracy of the estimate depends only on the number of random values (points) N. From a mathematical point of view, this is explained by the expression (1):

$$\int_a^b f(x)dx \approx \frac{b-a}{N} \cdot \sum_{i=1}^{N} f(u_i) \,. \tag{1}$$

The Monte-Carlo Method has several disadvantages: the first is its verification, i.e. the need to confirm the accuracy of numerical calculation results of RTD reliability indicators; the second is its duration, which consists of three components: the construction of a formal model, its verification and the conduct of a simulation experiment; and the lack of universality [10, 11].

Also requires highly qualified training of the operator (researcher). Therefore, this method of simulation is difficult, but it has the main advantage - authenticity.

A. Implementation of random variables

One of the most common hardware-software methods for obtaining random variables is the use of a pseudo-random number generator based on shift registers with linear feedback [5].

This method is implemented as a VI module (IP core for NI LabView FPGA) and can be used in various applications [12]. The implementation of a pseudo-random number generator based on linear feedback shift registers in the NI LabView is shown in Fig. 5.

When generating random numbers, the uniform distribution law of the random variable should be used [13].

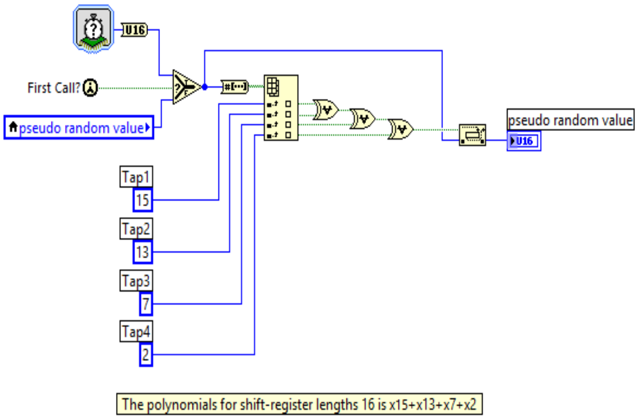

Fig. 5. Implementing a pseudo-random number generator based on linear feedback shift registers in the NI LabView

B. Creating a formal model

The formal model is one of the stages of the implementation of the Monte Carlo method in predicting the faultlessness characteristics of RTD. To build it, it is necessary to form a Scheme for Calculating the Dependability (SCD).

SCD can be presented in the form of a “Reliability Block Diagram” (RBD). RBD, in general, is a structural chain of a serial or parallel connection of IC, that displays failure criteria. An example of the image of the RBD is shown in Fig. 6.

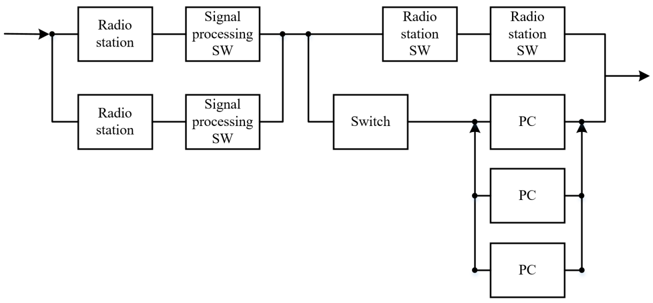

Fig. 6. Reliability Block Diagram

To simplify the verification of RBD of structurally complex RTD a “Group Tree” (GT) is formed, which consists of n-levels groups [14]. It should be noted that for GT the possibility of including the same IC in different paths is realized (Fig. 7).

According to Fig. 6 and Fig. 7, a certain n-level group consists of IC, the combination of which can be represented as Boolean logic using “AND”/“OR” logic elements for the purpose of unification (see Fig. 8).

Explanations for Fig. 8: the logical element “AND” represents a serial connection of IC and indicates the impossibility of obtaining a logical “1” at the output of this connection, since failure of any IC will lead to failure of the RTD.

Logical element “OR” displays a parallel connection of IC and indicates the possibility of obtaining a logical "1" at the output of this connection in the case of a feed to one of the inputs of a logical “0”, since failure of one IC will not lead to failure of RTD.

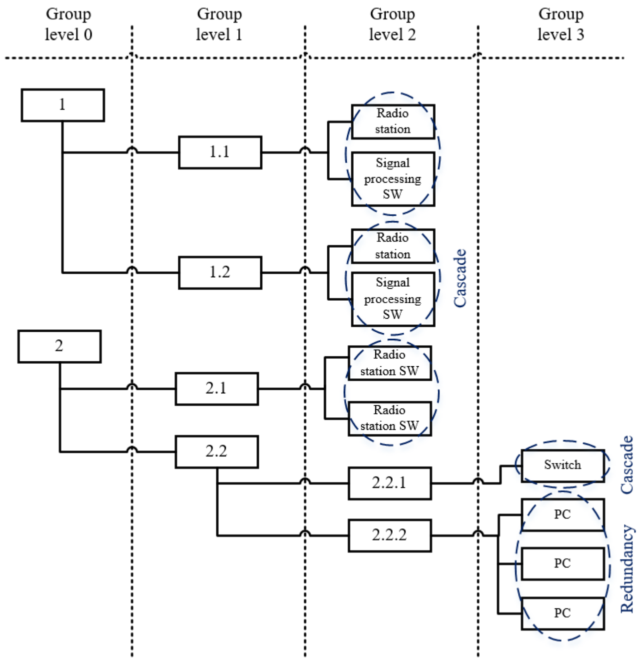

Fig. 7. The scheme for calculating the RTD reliability in the form of "Group tree"

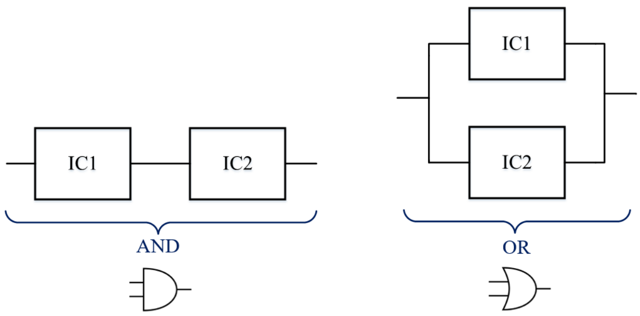

Fig. 8. Representation of the RTD components relationship in the form of a logical scheme

To achieve this view, you can use a common approach - the formation of “Fault Tree Analysis” (FTA) [15]. The essence of this approach is to build an acyclic oriented graph that determines the causal relationships of a system failure with the failures of its subsystems and elements, as well as other events and impacts (see Fig. 9).

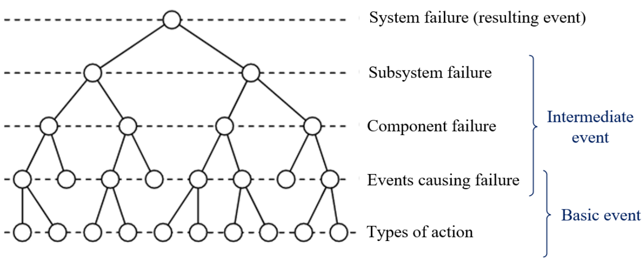

Fig. 9. Schematic illustration FTA

Formed SCD in the form of “Fault Tree” is due to the detailing of events related to system failures, its subsystems and elements (components) from the “effect” to the “cause” (i.e., “from top to bottom”) in order to find possible causes of their occurrence [15, 16].

Existing methods of working with FTA are aimed at implementing a static model, which imposes certain problems of quantitative analysis of dependability indicators by the considered method, because some events (impacts, failures) can occur during a certain time with a certain probability, and the time and sequence of their occurrence is not taken into account.

The use of the mathematical apparatus of Boolean logic allows us to simplify the conditions for the performance of complex RTD and the dependability calculation.

For example, if it is stated that the system is operable in the case of the operability of its two components "A" and "B", then it could be concluded that the system's operability (event "C") and the operability of components "A" and "B" (event "A" and event "B") are interconnected by a logical equation of operability:

$$C = A \wedge B \,, \tag{2}$$

where "∧" is logical operation "AND".

The logical equation of operability, for this case, is represented by the scheme of serial connection of elements A and B [17].

Therefore, it is recommended to use logical operators (vertices), taking into account the dependence of events, time relations, priorities (see Fig. 10).

Corner	**Name**	**Description**
	AND	Logical AND
	OR	Logical OR
	NAND	Logical NAND
	NOR	Logical NOR
	NOT	Logical NOT

Fig. 10. Logical operators (vertices)

By applying similar vertices to the failure tree, it is possible to calculate the following reliability characteristics: Failure Function - $Q(t)$, Reliability Function - $R(t)$, average number of failures N_0, etc.

Since the structural diagram can be represented as a logical diagram (see Fig. 8), then the application of FPGA technology is fair.

The sequence of representation of the object of study for reliability prediction is shown in Fig. 11.

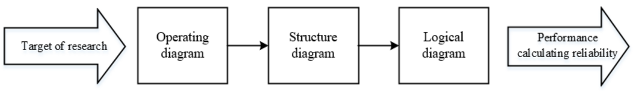

Fig. 11. Sequence of the object of study representation for predicting reliability

Explanations for Fig. 11: knowing the functional scheme of the object of study (RTD), it is possible to form a structural diagram, which, in turn, can be represented as a logical scheme (logical connection of the system components).

C. Statistical processing of simulation results

The method of statistical processing of simulation results consists of six main stages and is presented in the form of an IDEF$_0$-diagram (see Fig. 12).

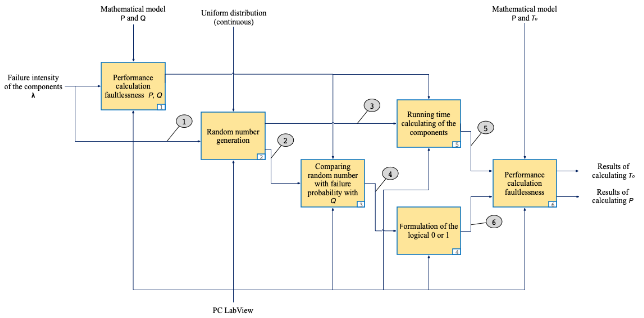

Fig. 12. Methods of statistical processing of simulation results

The formation of the initial data is based on the user's documentation, indicating the numerical values of the failure rates (λ) for each component of the RTD (system).

The first phase (see Fig. 12, Block 1) was aimed for calculating Failure Function of the IC (Q_i):

$$Q_i = 1 - \exp(-\lambda_i \cdot t) \,, \tag{3}$$

where t is operating time; i is IC number.

Further, the resulting numerical value Q_i is shown on the line [0; 1].

In the second stage (see Fig. 12, Block 2) the random numbers (x_i) were generated according to the uniform distribution (continuous).

The third phase (see Fig. 12, Block 3) was necessary to compared numerical value Q_i with the random generated number x_i according to the uniform distribution (continuous).

In the fourth stage (see Fig. 12, Block 4) failure or no failure of the IC was simulated. I.e. if the value of x_i gets into the interval [0; Q_i], failure component will simulate (logical "0" input comp.). But if the value of x_i gets into the interval [Q_i; 1], successful operation component will simulate no matter how long does it work (logical "1" input comp.).

The fifth phase (see Fig. 12, Block 5) is necessary to calculate the duration of the c work of the IC to failure (T_{Fi}). The expression (3) lead to the expression (4):

$$t_{Fi} = -\frac{\ln(x_i)}{\lambda_i} \,. \tag{4}$$

The final sixth stage (see Fig. 12, Block 6) permitted to estimate numerically the Reliability Function of RTD (system) in general, and Mean Operating Time to Failure of RTD (system), according to the expression:

$$P_s = \frac{n}{N} \,;\; T_{0s} = \frac{1}{N} \cdot \sum_{i=1}^{N} t_{Fi} \,. \tag{5}$$

where N is quantity of tests; n is number of tests with a positive result.

IV. Conducting a Virtual Experiment

The lightweight spacecraft electronic power supply was chosen as an object (RTD) in this scientific research. Fig. 13 represents the RBD of the lightweight spacecraft electronic power supply.

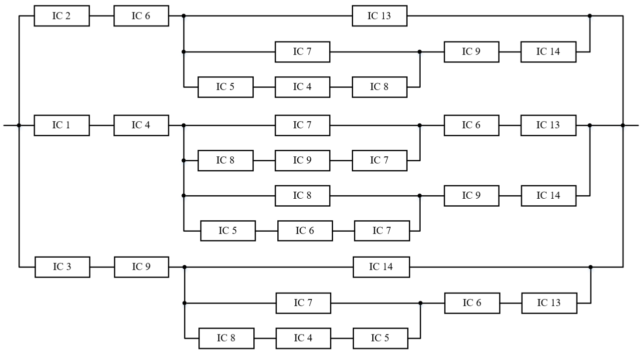

Fig. 13. The reliability block diagram of the lightweight spacecraft electrical power supply

Within virtual experiment a developed VI-module is used [18, 19]. Which demonstrates the work of the Monte Carlo Method for dependability predicting (reliability characteristics) structurally complex RTD.

Virtual experiment of the laboratory bench was performed with the aid of personal computer and software NI LabView for simulation of failures of reserved RTD. Fig. 14 represents, the front program panel.

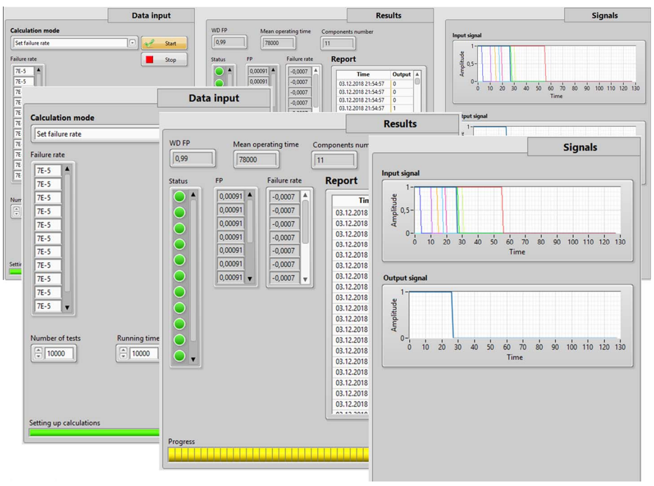

Fig. 14. Virtual appliance for predicting the faultlessness characteristics by reserved RTD

As a result of the experiment the values were obtained P_s = 0,99 (operating time = 50000 h.) and T_{0s} = 78000 h. for 10 thousand tests.

V. Conclusion

Thus, it could be concluded that the National Instruments toolbox allows you to create a laboratory bench for predicting the reliability of wireless devices using the simulation modeling. The use of such bench can be applicable not only in predicting wireless devices reliability in engineering practice, but also in the training of bachelors and masters of engineering directions.

References

[1] I. I. Aleksandrovich et al., “Estimation of Durability Indices of Integrated Microcircuit Communication Network”, in *Proc. 2016 International Siberian Conference on Control and Communications (SIBCON)*, Moscow, Russia, 2016. DOI: 10.1109/SIBCON.2016.7491837

[2] Y. G. Zaiko et al., “Simulation Model to Calculate the Indices of Reliability of Redundant Radio Electronic Systems”, *Dependability*, no. 3, pp. 8-17, Oct. 2016. DOI: 10.21683/1729-2646-2016-16-3-8-17

[3] S. A. Prashikin, “Programming Calculating Method Reliability Targets Restorable Facilities Redundant Groups by Monte-Carlo Method” (in Russian), *in Proc. 15th Scientific-Practical Seminar “New Information Technologies in Automated Systems*”, Moscow, Russia, 2012, pp. 250-252.

[4] V. V. Zhadnov and A. A. Iofin, “Comparative characteristics of the PC ASONIKA-K and reliability calculations programs”, in *Proc. 2014 International Conference “Modern Problems of Radio Engineering, Telecommunications and Computer Science” (TCSET’2014)*, Lviv, Ukraine, 2014, pp. 226-228.

[5] B. Schneier, *Applied Cryptography: Protocols, Algorithms and Source Code in C, (20th ed.),* Hoboken, New Jersey: John Wiley & Sons, 2017

[6] National Instraments. (2016, May). *User Guide And Specifications NI MyRIO-1900* [Online]. Available: URL: http://www.ni.com/pdf/manuals/376047c.pdf

[7] National Instraments. (2018, Jan.). *MyRIO - trining device for engineering embedded systems* [Online]. Available: URL: http://www.ni.com/ru-ru/shop/select/myrio-student-embedded-device

[8] V. Y. Zotov, “New Generation Software Design Singularity of PLD with FPGA by XILINX Company” (in Russian), *Components & Technologies*, no. 12, pp. 17-24, Dec. 2010

[9] G. Fishman, *Monte Carlo: Concepts, Algorithms, and Applications*, New York: Springer, 1995

[10] V. N. Zadoroznyi, S. A. Rafalovich, “Equation Solution in Switching Function on GPSS WORLD” (in Russian), *in Proc. Students Scientific-Practical Conf. “Automated systems of information processing and administration in ASRWS*”, Omsk, Russia, 2007, pp. 31-34

[11] V. V. Zhadnov and A. N. Tikhmenev, “Simulation Modeling in Estimating Reliability of Fail-Safe Electronic Equipment”, *Dependability*, no. 1, pp. 44-54, Apr. 2013. DOI: 10.21683/1729-2646-2013-0-1-32-54

[12] BetaCommunityCo. (2017, Jan. 27). *LV FPGA Pseudo Random Number Generator* [Online]. Available: URL: https://www.forums.ni.com

[13] *Statistical methods. Determination Rules and Methods for Calculation of Statistical Characteristics Based on Sample Data. Part 1. Normal Distribution*, National Standard of Russian Federation 50779.21, 2004

[14] V. V. Zhadnov et al., *Information Technology Reliability Providing of Electronic Means of an Earth- and Space-Based Systems: Science Publication (in Russian)*, Yekaterinburg: Fort Dialog-Iset Ltd, 2012

[15] *Dependability in Technics. Dependability Prediction. Basic Principles*, Interstate Standard 27.301, 1995

[16] V. I. Patrushev, *Reliability and Effectiveness in Equipment. Reliability Project Analysis (in Russian)*, Moscow, Russia: Mashinostroenie, 1988.

[17] A. V. Stroganov et al., “Review of Computer Software for Reliability Prediction of Complex Technical System” (in Russian), *Components & Technologies*, no. 5, pp. 183-190, May 2007

[18] P. S. Korolev “Reliability Prediction of Complex Radio Devices with the Possibility of Using Hardware and Software Platform NI MyRio” (in Russian), *in Proc. 21th Scientific-Practical Seminar “New Information Technologies in Automated Systems*”, Moscow, Russia, 2018, pp. 255-259.

[19] P. S. Korolev “Possibility of Implementing the Method of Fault Tree for Statistical Models in PC Multisim and LabView” (in Russian), *in Proc. Scientific-Technical Conference of Young Specialists “Electronic and Electromechanical Systems and Devices*”, Tomsk, Russia, 2018, pp. 295-297.