SPICE Simulation of Total Dose and Aging Effects in MOSFET Circuits

Petrosyants K.O. [1,2], Kharitonov I.A. [2]
[1]*National Research University Higher School of Economics*
(Moscow Institute of Electronics and Mathematics)
[2]*Scientific Research Institute of Advanced Materials and Technology, Moscow, Russia*
E-mail: ikharitonov@hse.ru

Abstract

An extended version of MOSFET RAD SPICE model providing combined account for aging and total dose effects is described. The model uses summation of radiation induced (depending on dose rate, irradiation time, electrical bias) oxide and interface traps densities and interface densities produced by hot electrons to calculate MOSFET characteristics. The model was built using macromodeling approach, standard SPICE models for MOSFETs (BSIMSOI or EKV) and model parameters dependences on electrical stress and total dose irradiation factors. The developed model accounts for enhanced degradation due to combined TID and electrical stress conditions.

1 Introduction

As it is well known, aging (parameters degradation) of electronic components is important factor that is necessary to account for electronic equipment in design phase. From the other hand there are industry areas that need for electronics that can operate reliably in harsh environments, including low, and high temperatures, radiation influence. These areas include equipment for avionics, satellites, deep space, nuclear particle detectors, nuclear reactors, etc. [1]. The mentioned ambient factors (temperature and total irradiation dose (TID)) change components parameters that can accelerate the aging process: channel hot carrier effects (CHC) and negative bias temperature instability (NBTI) [2-4]. Temperature influence on MOSFET aging process is known and well described. To design circuits and systems which are radiation hard and reliable during their live, the models are need that can account for radiation and aging (due to hot carriers) effects (see [2]-[4] and others). Interaction between irradiation and hot carriers effects for thick oxides was analyzed in early works [4], [5]. Works [2], [3] investigated the mentioned effects in modern 130…150 nm MOSFETs. However questions of modeling aspects of combined TID and aging effects were not described enough.

2 Approaches to account for TID and hot carrier effects in MOSFETs characteristics modeling

As it well known, irradiation of MOSFET structure results to holes generation in oxide layers and interface states generation in Si-oxide interfaces. These effects result to threshold voltage shift, carriers mobility degradation, subthreshold slope decrease. From the other hand, hot electrons which are responsible for MOSFETs aging also create interface traps, with the similar effects on MOSFET characteristics as for radiation influence.

So for NMOS FETs negative interface traps ΔN_{it_stress} after electrical stress partially compensate positive oxide charges ΔN_{ot_D} and reduce threshold voltage shift after combined TID and hot electrons impacts. However summed ΔN_{it_stress} and ΔN_{it_D} result to increased (in comparison with only TID or hot carrier effects) degradation of carrier mobility and subthreshold swing ([2]-[5]). Furthermore, drain leakage current may substantially increase after TID irradaiation. For PMOS FETs positive interface traps ΔN_{it_stress} after electrical stress are summated with TID induced positive interface traps ΔN_{it_D} and increase threshold voltage shift, mobility degradation and subthreshold swing after combined TID and hot electrons impacts. So combined effects of TID and electrical stress result to increased MOSFET characteristics degradation and reduce the MOSFET live time. For cases when irradiation results to enhanced hot electron degradation the integrated effects may be much larger [2] and component live time smaller .

978-1-5386-5710-2/18/$31.00 ©2018 IEEE

Paper [6] presents reliability simulation flow with SPICE using MOSFET model parameter dependencies on generated interface traps after electric stress (the well known equations for threshold voltage and mobility dependencies on interface traps densities were used).

Paper [4] presented model for long channel (2 mkm) MOSFET for joined account of total dose and electrical stress effects. In this paper channel damages was divided to specific regions of MOSFET channel: the part which accounts for radiation damage and part nearly drain which accounts for hot carrier damage. However questions of time and dose dependences of TID effects and time dependences of stress effects were not considered.

Paper [3] presented a physics-based compact modeling approach that incorporates the impact of total ionizing dose and stress-induced defects. Authors utilized *calculations of surface potential* to capture the charge contribution from oxide trapped charge and interface traps and to describe their impact on MOS electrostatics and device operating characteristics as a function of ionizing radiation exposure and aging effects. They assumed linear summing of radiation and hot carrier induced charges and interface traps (for 180 nm CMOS process). However questions of modeling of oxide trapped charge and interface traps due to TID and electrical stress time were not considered enough.

Paper [2] focuses on investigation of electrical stresses on n-channel MOSFETs performed after irradiation with X-ray up to 136 Mrad(SiO2) in different bias conditions. Outhors showed that irradiation negatively affects (enhances) the degradation during subsequent hot carrier injection. Using TCAD simulation they showed that an enhanced impact ionization at the bulk-STI interfaces is due to radiation-induced trapped charge and defects. So the resulting degradation after irradiation and electrical stress exceeds sum of their separate contributions for narrow MOSFETS. They concluded that for harsh-radiation environments hot-carrier lifetime may be decreased due to irradiation.

3 Extension of our model RAD-SPICE model to account for the aging effects

We think that the physics-based compact modeling approach [3] is convenient for MOSFET characteristics simulation for TID and electrical stress conditions by itself, but it is difficult to use this approach for widely used standard BSIM, BSIM SOI SPICE models. Furthermore, the authors of [3] did not use the defect densities dependencies on time, dose, voltage etc. It is not convenient for circuit designer and doesn't allow to account for aging time, dose rate and other parameters of MOSFET working conditions. From the other hand earlier we developed RAD SPICE models for MOSFETs [7], [8] (and others) which use standard models and allow to account for TID effects, including dose rate, irradiation time, electrical conditions. The mentioned models use oxide trapped holes N_{ot_D} and interface traps N_{it_D} densities, and their dependencies on the mentioned irradiation factors. So as aging effects (hot carrier injection and NBTI) result to gate oxide and interface traps generation too, it is convenient to combine these defect densities and to provide integrated account for TID and aging effects using our model. So in present paper we made the text step and extended our models possibilities by including interface traps densities N_{it_stress} caused by electrical stress (aging effects). The novelty of the presented model for MOSFET is possibility to account for combined time, dose rate factors for TID and time factor for electrical stress effects in CMOS circuit (SPICE) simulation flow.

As it was described in our papers [8], [9] inside the model we use concentrations of gate oxide charge and interface traps densities to account for the nonlinear dependencies of the threshold voltage of MOSFET, channel mobility, subthreshold slope on irradiation time, dose rate, irradiation level using the known equations. So to account for hot electron effects we modified our equations.

Threshold voltage VTH0 of main MOSFET is described by the usual equation:

$$VTH0(D, stress\_time) = VTH0(0) - \frac{\Delta N_{ot\_D}(D)q}{C_{ox}} \pm \frac{\left(\Delta N_{it\_D}(D) \pm \Delta N_{it\_stress}(stress\_time)\right)q}{C_{ox}}, \quad (1)$$

where *VTH0(0)* –threshold voltage of MOSFET before irradiation and stress;

C_{ox} – gate oxide capacitance.

Threshold voltage of parasitic MOSFET (describing leakage current after TID impact) is described by the usual equation [8].

The *MOSFET mobility* (SPICE model parameter) dependence on TID and hot carrier effects is described by:

$$U0(\mathrm{D}, stress\_time) = \frac{U0(0)}{1 + \alpha_{it}\left(N_{it\_D}(D) + N_{it\_\mathrm{stress}}(stress\_time)\right)}, \quad (2)$$

where U0(0) –channel mobility value before irradiation and electrical stress,

α_{it} – fitting coefficients.

I_d-V_{gs} subthreshold slope dependence on TID and hot carrier effects is described by correction of model parameter c_{it}:

$$C_{it}(D, stres\_time) = \\ = k_{it} \cdot q \cdot (\Delta N_{it}(D) + \Delta N_{it}(stress\_time)). \quad (3)$$

In the above equations:

$\Delta N_{ot\_D}(D)$, $\Delta N_{it\_D}(D)$ - radiation induced, dose rate, time and dependent concentrations of gate oxide charge and interface traps densities, correspondingly;

$\Delta N_{it\_stress}(stress\_time)$ - hot carriers induced interface traps density.

Oxide charge $\Delta N_{ot\_D}(D)$ and interface traps densities $\Delta N_{it\_D}(D)$ dependencies on dose rate, irradiation time and electrical bias are described in our papers [7],[8] and are not considered here.

For interface trap densities ΔN_{it_stress} we use the usual dependencies [11] on stress time and electrical bias in the MOSFET structure:

$$\Delta N_{it\_stress}(stress\_time) = f(\mathrm{E}) \cdot stress\_time^{k} \quad (4)$$

where *f(E)* – function describing interface traps generation in dependence on electrical conditions and features of MOSFET structure,

k – fitting coefficient (usually 0.5…0.75) (see [11] and others).

The mentioned model parameters are define from the characteristics of MOSFETs after TID and electrical stress impact by our usual extraction methods and automated measuring system [12].

4 MOSFET characteristics simulation with account for TID and aging effects

As an example we used 130 nm MOSFET characteristics after 500krad (Si) irradiation from [10], and some others; MOSFET characteristics after 10 000 seconds - from work [11].

As it is seen from Fig. 1 TID results to large increase of drain leakage of NMOSFET (because of shallow trench insulation) and small shift of threshold voltage. For PMOSFET devices TID irradiation results to small (20…30 mV) increase of threshold voltage. The mentioned characteristics were used to define $\Delta N_{ot\_D}(D)$, $\Delta N_{it\_D}(D)$, $\Delta N_{it\_stress}(stress\_time)$ dependence parameters. The simulated I_d-V_{gs} characteristics are presented in Figures 2 and 3.

For simplicity we assume linear summation of TID and electrical stress induced oxide charge and interface traps.

5 Application of the developed SPICE model for CMOS circuit simulation with combined account for TID and aging effects

We illustrate combined influence of TID and electrical stress effects on CMOS circuit by clearly evident example - CMOS inverter with transistors sizes L=0.15 μm, W=0.33 μm.

The simulated characteristics are presented in Fig 4: (a)- for TID values 0, 500krad, 1000 krad; (b)- for unirrradiated circuit for stress time values 0 , 10 000 sec; (c) – for combined effects of TID values 0, 500krad and stress time values 0 , 10 000 sec. The calculated dynamic parameters of the circuit are presented in Tabl. 1. It is seen that combined effects of TID and hot carrier on CMOS inverter circuit result to much more degradation of transient characteristics in comparison with only TID or hot carrier effects.

Table 1. Simulated dynamic characteristics of 130 nm CMOS inverter before and after TID irradiation 500 krad and electrical stress of 10 000 sec.

Conditions	t_{rise}, ns	t_{fall}, ns	t_{delay}^{01}, ns	t_{delay}^{10}, ns
D=0, stress time=0	0.09	0.02	0.04	0.03
D=500 krad, stress time=0	0.14	0.022	0.055	0.04
D=0, stress time= 10 000 sec.	0.15	0.04	0.1	0.05
D=500 krad, stress time= 10 000 sec.	0.24	0.055	0.13	0.065

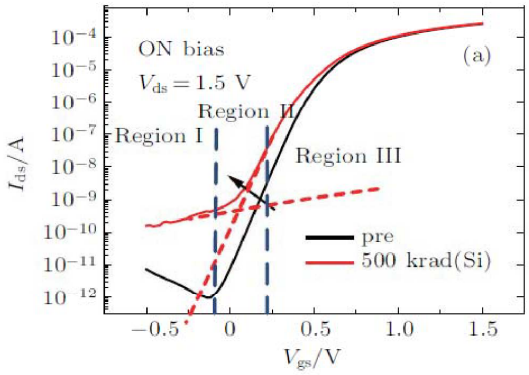


Fig. 1 Measured [10] I_d-V_{gs} characteristics of 130 nm NMOSFET before and after 500 krad TID

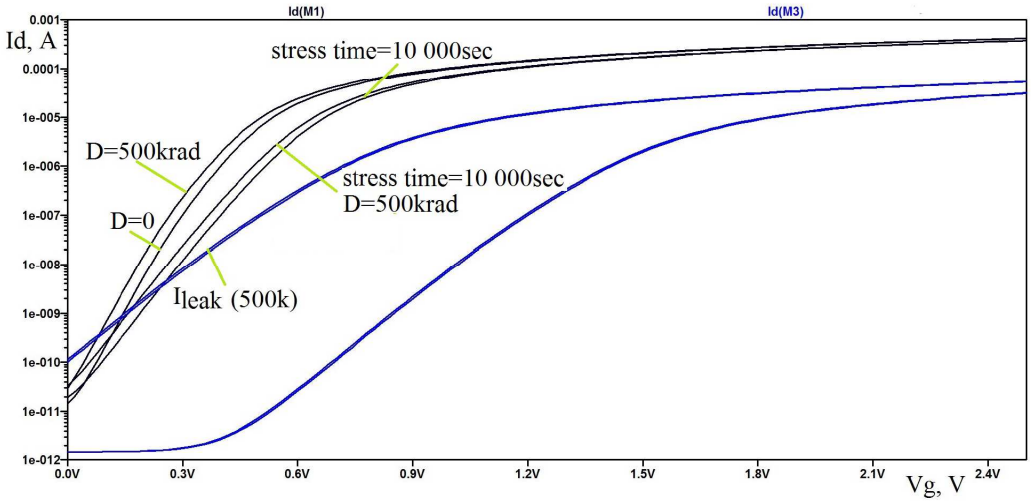


Fig. 2 Simulated with our model I_d-V_{gs} characteristics of 130 nm NMOSFET before and after 500 krad TID and after 10 000 sec stress; before and after 500 krad TID alone and after 10 000 sec stress alone

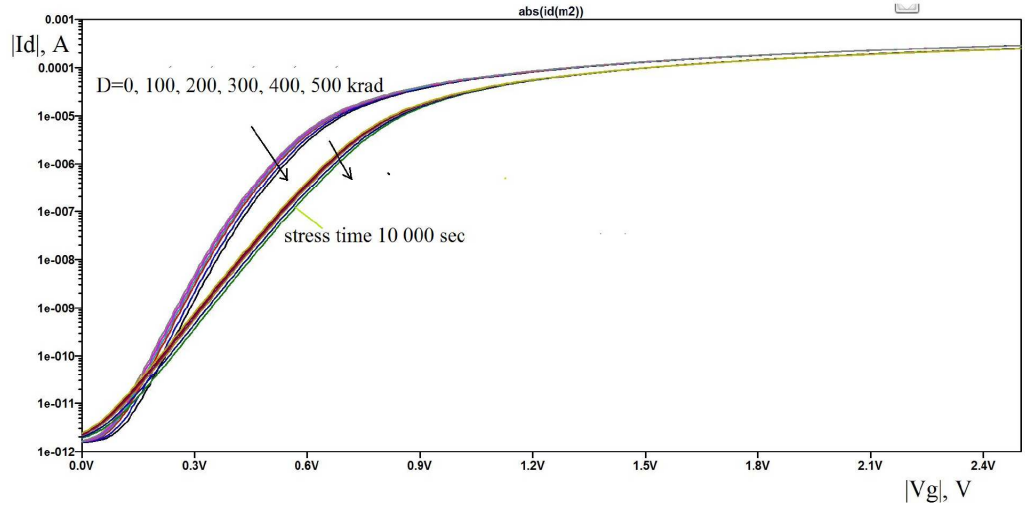
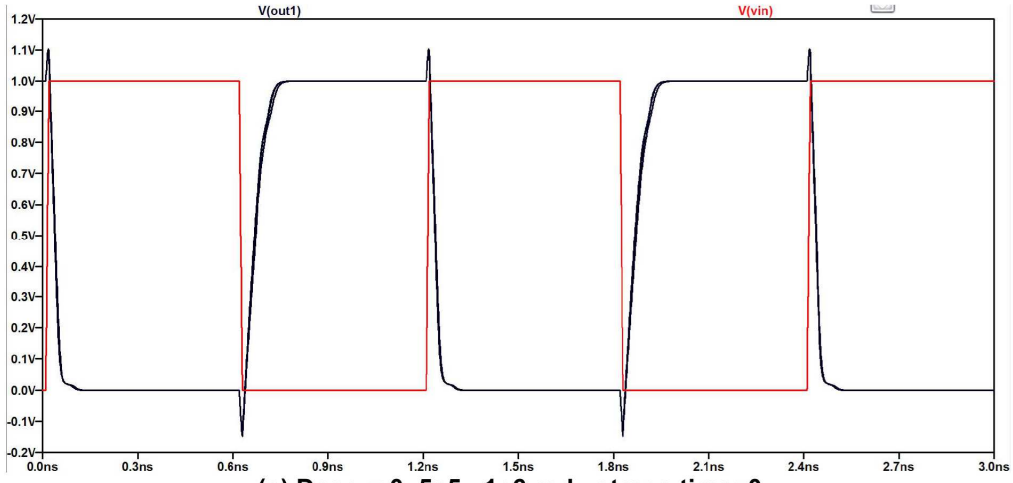
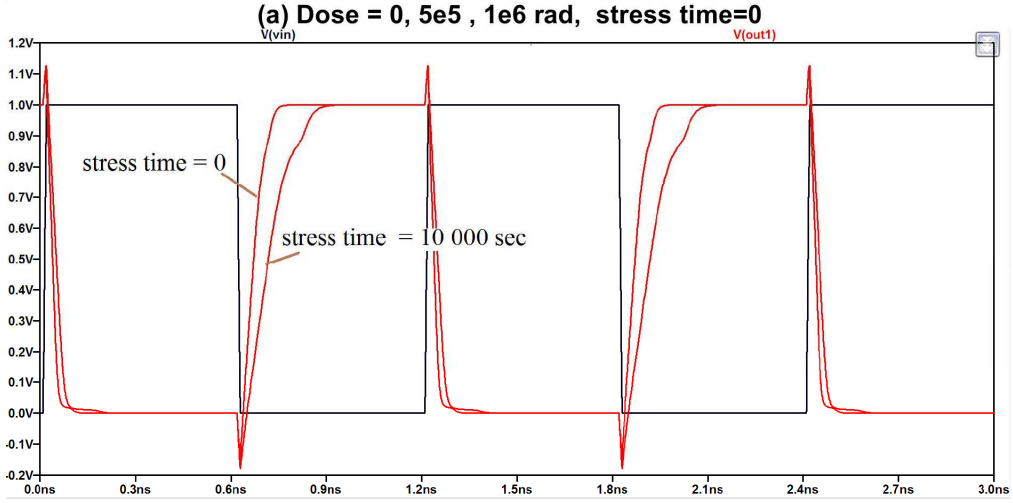


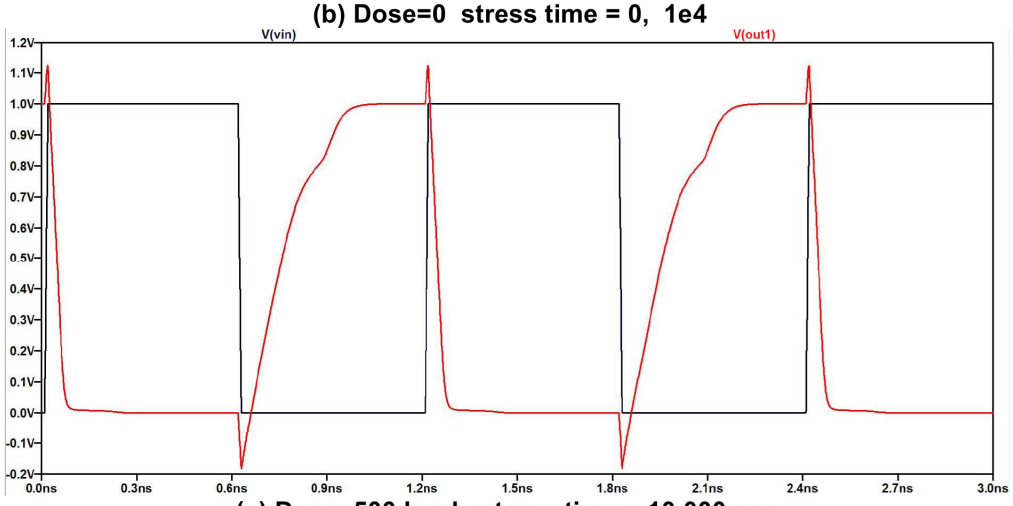
Fig. 3. Simulated with our model I_d-V_{gs} characteristics of 130 nm PMOSFET after doses 0…500 krad TID and stress time 0… 10 000 sec



(a) Dose = 0, 5e5 , 1e6 rad, stress time=0



(b) Dose=0 stress time = 0, 1e4



(c) Dose=500 krad, stress time = 10 000 sec.

Fig. 4. Simulated with our model transient characteristics of CMOS inverter with account for TID effects (0, 500krad, 1000krad) (a); with account for hot carrier effects (0, 10 000 sec) (b); with account for combined TID (500krad) and hot carrier (stress time 10 000 sec) effects (c)

6 Conclusions

The extended version of our RAD SPICE model for MOSFET was presented for hardened CMOS ICs automated design with combined account for TID and aging (due to hot carries) effects. The macromodeling approach with model parameter dependencies on oxide charge and interface traps densities due to radiation level and electrical stress time were used together to account for their combined influence. The extended version of the model allows to account for dose rate, time for TID impact and electrical mode and time for aging effects in SPICE simulation flow of hardened CMOS circuits.

Simulation results confirmed that combined influence of the mentioned effects results to enhanced degradation of MOSFET characteristics and CMOS circuits and should be taken into account for analysis of live time of reliable electronic circuit for harsh environment.

The next step may be more detailed simulation of nonlinear interaction of TID and hot carrier effects for small (narrow) MOSFET structures.

The present article was prepared within the state assignment of Ministry of Education and Science of the Russian Federation, project no. 8.9382.2017/8.9.

References

[1] "Improved Design of Radiation Hardened, Wide-Temperature Analog and Mixed-Signal Electronics Project"., NASA Project, [https://catalog.data.gov/ dataset/improved-design-of-radiation-hardened-wide-temperature-analog-and-mixed-signal-electronics].

[2] Marco Silvestri, Simone Gerardin, Alessandro Paccagnella, Federico Faccio, "Hot Carrier Stress on Irradiated 130-nm NMOSFETs", *IEEE Trans. on Nucl. Scie.*, vol. 55, N 4, 2008, pp. 1960- 1967.

[3] I. Sanchez Esqueda, H. J. Barnaby, and M. P. King, "Compact Modeling of Total Ionizing Dose and Aging Effects in MOS Technologies", *IEEE Trans. on Nucl. Scie.*, vol.62, N4, 2015, pp. 1501-1516.

[4] J. D. McBrayer, R. A. Pastorek and R. V. Jones, "A model describing hot-carrier and radiation effects in MOS transistors", *IEEE Trans. on Nucl. Scie.*, vol. NS-34, N6, 1987, pp. 1647-1654.

[5] J. D. McBrayer, D. M. Fleetwood, R. A. Pastorek, and R. V. Jones, "Correlation of hot-carrier and radiation effects in MOS transistors", *IEEE Trans. Nucl. Sci.*, vol. NS-32, no. 6, Dec. 1985, pp. 3935–3939.

[6] Mehdi Kamal, Qing Xie, Massoud Pedram, Ali Afzali-Kusha, Saeed Safari, "An Efficient Reliability Simulation Flow for Evaluating the Hot Carrier Injection Effect in CMOS VLSI Circuits", *Proc. of 2012 IEEE 30th International Conference on Computer Design (ICCD)*, 2012.

[7] Kharitonov I.A., "Multi level methodology for CMOS circuit design taking into account thermal and radiation effects". *Proc. of International Scientific – Practical Conference «INFORMATION INNOVATIVE TECHNOLOGIES»*, Prague, April 2017, pp. 309-316.

[8] Konstantin O. Petrosyants, Kharitonov I. A., Sambursky L. M., "SOI/SOS MOSFET Universal Compact SPICE Model with Account for Radiation Effects", *Proc. of 2015 IEEE Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS-2015),* 2015. Bologna, Italy, pp. 305-308.

[9] Kharitonov I. A., "Electro-Thermo-Rad SPICE models for SOI/SOS MOSFETs", *Proc. of the XV IEEE East-West Design & Test Symposium (EWDTS'2017).* Piscataway : IEEE, 2017. pp. 1-8.

[10] Q. Zheng *et al,* "Direct measurement and analysis of total ionizing dose effect on 130 nm PD SOI SRAM cell static noise margin", *Chinese Phys. B* **26,** 2017 096103

[11] M. Silvestri, S. Gerardin, A. Paccagnella, F. Faccio, L. Gonella, "Channel Hot Carrier Stress on Irradiated 130-nm NMOSFETs", *IEEE Trans. on Nucl. Sci* .Vol. 55, N. 4, 2008, pp.1960-1967.

[12] Petrosyants K. O., Kharitonov I. A., Sambursky L. M., "Hardware-Software Subsystem for MOSFETs Characteristic Measurement and Parameter Extraction with Account for Radiation Effects", *Advanced Materials Research.* 2013. Vol. 718–720. pp. 750-755.