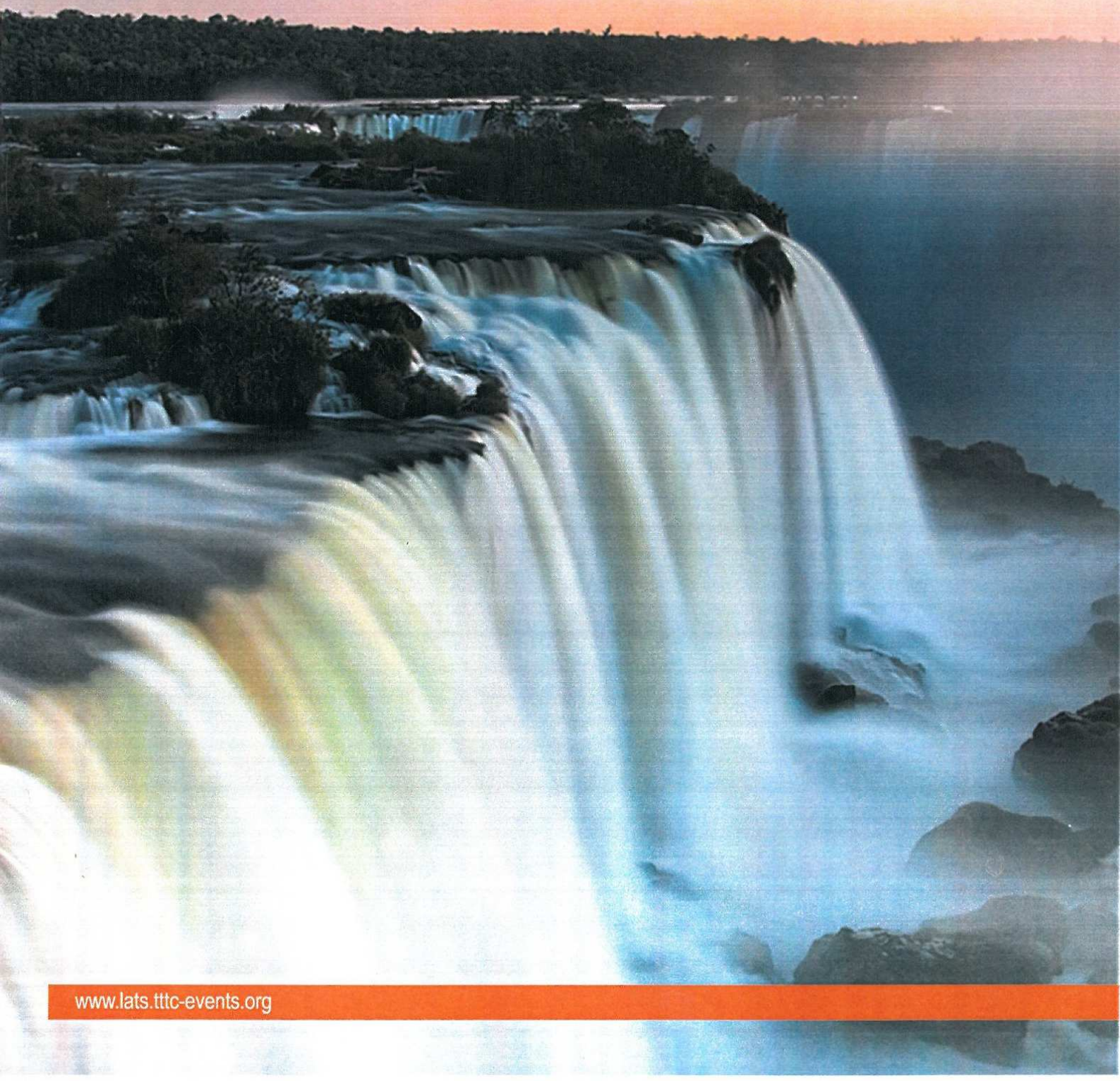
LATS2016

17th IEEE Latin-American Test Symposium

Foz do Iguaçu, Brazil, 6th - 8th April 2016

TTEP Day 9th April 2016



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Wednesday, 6th April 2016

08:00 - 09:00 Registration

09:00 - 09:20 Opening Session

General Chairs:
Letícia Maria Bolzani Poehls – PUCRS, Brazil;
Yervant Zorian – Synopsys, USA
Program Chairs:
Matteo Sonza Reorda – Politecnico di Torino, Italy;
Tiago Balen – UFRGS, Brazil

09:20 - 10:00 Keynote Talk

The Hype, Myths, and Realities of Testing 2.5D/3D Integrated Circuits

Krishnendu Chakrabarty – Duke University, USA
Chair: Bernd Becker – University of Freiburg, Germany

10:00 - 10:20 Coffee Break

10:20 - 11:00 Session 1

Fault Tolerant Architectures

Chair: Mario Schölzel – IHP, Germany

On the Analysis of the Effects of Soft Errors on Compression Algorithms
Massimo VIOLANTE, Matteo SONZA REORDA, Serhiy AVRAMENKO (Politecnico di Torino, Italy), G. FEY (DLR, Germany)

A Comprehensive Approach to Fault Tolerance (Invited presentation)
Zoran STAMENKOVIC, Vladimir PETROVIC (IHP, Germany)

11:00 - 12:00 Session 2

Microprocessor Test and Reliability

Chair: Fernanda Kastensmidt – UFRGS, Brazil

Auxiliary IP Blocks for Early Dependability Analysis of Small Processor based Systems
Jorge BARBOZA, Jose BASUALDO, Julio PEREZ (Universidad de la Republica, Uruguay)

Dependability Evaluation of COTS Microprocessors via On-Chip Debugging Facilities
Jose ISAZA-GONZALEZ, Alejandro SERRANO-CASES (University of Alicante, Spain), Felipe RESTREPO-CALLE (Universidad Nacional de Colombia, Colombia), Sergio CUENCA-ASENSI, Antonio MARTÍNEZ-ÁLVAREZ (University of Alicante, Spain)

A Comprehensive Software-Based Self-Test and Self-Repair Method for Statically Scheduled Superscalar Processors
Mario SCHÖLZEL (IHP and University of Potsdam, Germany)

12:00 - 13:40 Lunch

13:40 - 14:20 Invited Talk

Accessing On-Chip Instruments through the System's Life-Time

Erik Larsson – Lund University, Sweden
Chair: Francisco Russi – Synopsys, USA

14:20 - 15:20 Session 3

Fault Modeling and Simulation

Chair: Victor Champac – INAOE, Mexico

A Probabilistic Model for Stuck-On Faults in Combinational Logic Gates
Rafael SCHIVITTZ (FURG, Brazil), Denis FRANCO (UFPel, Brazil), Cristina MEINHARDT (FURG, Brazil), Paulo BUTZEN (FURG, Brazil)

Fault model qualification by assertion mining
Graziano PRAVADELLI, Alessandro DANESE (University of Verona, Italy)

A Control Path Aware Metric for Grading Functional Test Vectors
Kelson GENT (Virginia Polytechnic Institute and State University, USA), Michael HSIAO (Virginia Tech, USA)

15:20 - 15:40 Coffee Break

15:40 - 16:40 Session 4

Fault Tolerance in SoCs and NoCs

Chair: Robert Aitken – ARM, USA

On the Consolidation of Mixed Criticalities Applications on Multicore Architectures
Massimo VIOLANTE, Stefano ESPOSITO, Serhiy AVRAMENKO (Politecnico di Torino, Italy)

Using Traffic Monitors to Tolerate Multiple Faults in 3D NoCs
Anelise KOLOGESKI, Henrique Colao ZANUZ, Fernanda KASTENSMIDT (UFRGS, Brazil)

On-line Fault Classification and Handling in IEEE 1687 Based Fault Management System for Complex SoCs
Konstantin SHIBIN (Tallinn University of Technology, Estonia), Artur JUTMAN (Testonica Lab, Estonia), Sergei DEVADZE (Tallinn University of Technology, Estonia)

16:40 - 17:40 Session 5

NBTI Modeling and Mitigation

Chair: Zoran Stamenkovic – IHP, Germany

Gate-Level Modelling of NBTI-Induced Delays under Process Variations
Thiago Santos COPETTI, Guilherme MEDEIROS, Leticia BOLZANI POEHLS, Fabian VARGAS (PUCRS, Brazil), Sergei KOSTIN, Maksim JENIHHIN, Jaan RAIK, Raimund UBAR (Tallinn University of Technology, Estonia)

A Methodology to Assure Circuit Reliability at Reduced Power Consumption using Dual Supply Voltage
Freddy FORERO, Andres GOMEZ, Victor CHAMPAC (INAOE, Mexico)

Analyzing NBTI Impact on SRAM Cells with Resistive-Open Defects
Marco MARTINS, Guilherme CARDOSO MEDEIROS, Thiago Santos COPETTI, Fabian VARGAS, Leticia Maria BOLZANI POEHLS (PUCRS, Brazil)

17:40 - 18:40 Panel 1

Radiation Facilities in South America

Organizers: Raoul Velazco (INPG, TIMA, France) and Fernanda Kastensmidt (UFRGS, Brazil)

panelists: Raoul VELAZCO (INPG, TIMA, France), Nahuel VEGA (CONAE, Argentina), Fernanda KASTENSMIDT (UFRGS, Brazil) and Fabian VARGAS (PUCRS, Brazil)

18:40 - 19:20 LA TTTC Meeting *

* open, optional activity

20:00 - 22:00 Welcome Cocktail

Thursday, 7th April 2016

09:00 - 09:40 Invited Talk

Known Unknowns - Knowledge in the Presence of Unknowns

Bernd Becker - University of Freiburg, Germany

Chair: Hans-Joachim Wunderlich – University of Stuttgart, Germany

09:40 - 10:20 Session 6

Soft Errors in Memory and Processors

Chair: Fabian Vargas – PUCRS, Brazil

Evaluating the Effects of Single Event Upsets in Soft-core GPGPUs
Werner NEDEL, Fernanda KASTENSMIDT (UFRGS, Brazil), José AZAMBUJA (FURG, Brazil)

Hybrid Soft Error Mitigation Techniques for COTS Processor-based Systems
Eduardo CHIELLE (UFRGS, Brazil), Boyang DU (Politecnico di Torino, Italy), Fernanda KASTENSMIDT (UFRGS, Brazil), Sergio CUENCA-ASENSI (University of Alicante, Spain), Luca STERPONE, Matteo SONZA REORDA (Politecnico di Torino, Italy)

10:20 - 10:40 Coffee Break

10:20 - 11:00 Poster Session

Chair: Leticia Maria Bolzani Poehls – PUCRS, Brazil

On Automatic Software-Based Self-Test Program Generation Based on High-Level Decision Diagrams
Artjom JASNETSKI, Raimund UBAR, Anton TSERTOV (Tallinn University of Technology, Estonia)

A Deep Analysis of SEU Consequences in the Internal Memory of LEON3 Processor
Raoul VELAZCO, Afef KCHAOU (TIMA, France), Wajih EL HADJ YOUSSEF (LEME, Tunisia), Fraidy BOUESSE, Pablo RAMOS (TIMA, France)

Software Errors Analysis at the Zynq SoC ARM Embedded Processor
Gennaro RODRIGUES , Fernanda KASTENSMIDT (UFRGS, Brazil)

Reliability Analysis of Majority Voters under Permanent Faults
Eduardo LIEBL, Cristina MEINHARDT, Paulo BUTZEN (FURG, Brazil)

Single Trojan Injection Model Generation and Detection
Daniel SAAB (CWRU, USA), Jacob ABRAHAM (University of Texas, USA), Harini BHAMIDIPATI (LSI Logic, USA)

Checksum Based Error Detection in Linearized Representations of Non Linear Control Systems
Suvadeep BANERJEE, Abhijit CHATTERJEE (Georgia Institute of Technology, USA), Jacob ABRAHAM (University of Texas, USA)

11:00 - 12:00 Session 7

Radiation Effects and Mitigation

Chair: Raoul Velazco – INPG and TIMA, France

Radiation Effects in Low Power and Ultra Low Power Voltage References
Daniel FUSCO, Tiago BALEN (UFRGS, Brazil)

Fault Simulation in Radiation-Hardened SOI CMOS VLSIs using Universal Compact MOSFET Model
Konstantin PETROSYANTS, Lev SAMBURSKY, Igor KHARITONOV, Boris LVOV (Moscow Institute of Electronics and Mathematics of National Research University "Higher School of Economics", Russia)

Performance Evaluation of Radiation Hardened Analog Circuits based on Enclosed Layout Geometry
Guilherme CARDOSO, Tiago BALEN (UFRGS, Brazil)

12:00 - 13:00 Panel 2

Hardware Security and Trust

Organizers: Ramesh Karri (Polytechnic School of Engineering, New York University, USA) and Ozgur Sinanoglu (New York University in Abu Dhabi, UAE)

Coordinator: Fabian Vargas (PUCRS, Brazil)

Panelists: Michail MANIATAKOS (New York University Abu Dhabi, UAE), Krishnendu Chakrabarty (Duke University, USA), and Yervant Zorian (Synopsys, USA)

13:00 - 14:30 Lunch

14:30 - 18:30 Social Event

20:30 - 23:30 Gala Dinner

Friday, 8th April 2016

09:00 - 09:40 Invited Talk

Transforming Nanodevices into Nanosystems: The N3XT 1,000X

Subhasish Mitra – Stanford University, USA
Chair: Pierre-Emmanuel Gaillardon – University of Utah, USA

09:40 - 10:20 Session 8

Defect Based Test and Silicon Validation

Chair: Erik Larsson – Lund University, Sweden

Comparative study of Bulk, FDSOI and FinFET technologies in presence of a resistive short defect
Amit KAREL, Mariane COMTE, Jean-Marc GALLIERE, Florence AZAIS, Michel RENOVELL (LIRMM, France)

On-Silicon Validation of a Benchmark Generation Methodology for Effectively Evaluating a Combinational Cell Library Design
Mauricio CARVALHO, Mauricio ALTIERI, Lauro PURICELLI (UFRGS, Brazil), Paulo BUTZEN (FURG, Brazil), Renato RIBAS, Eric FABRIS (UFRGS, Brazil)

10:20 - 10:40 Coffee Break

10:40 - 11:40 Session 9

Embedded Systems and Software Reliability

Chair: Graziano Pravadelli – University of Verona, Italy

A Framework for Early Functional Verification of Embedded Software Combining Virtual Platforms and Bounded Model Checking
Rogerio PALUDO, Djones LETTNIN (UFSC, Brazil)

Soft Error Analysis in Embedded Software Developed with & without Operating System
Luiz CASAGRANDE, Fernanda KASTENSMIDT (UFRGS, Brazil)

A HW-dependent Software Model for Cross-Layer Fault Analysis in Embedded Systems
Christian BARTSCH, Carlos VILLARRAGA, Dominik STOFFEL, Wolfgang KUNZ (University of Kaiserslautern, Germany)

11:40 - 12:20 Special Session 1

Dependable MPSoCs

Organizer: Fernando Gehm Moraes, (PUCRS, Brazil)

Dependable On-Chip Infrastructure for Dependable MPSOCs
Michael A. KOCHTE, Hans-Joachim WUNDERLICH (University of Stuttgart, Germany)

A Layered Approach for Fault Tolerant NoC-Based MPSoCs
Eduardo WACHTER, Francisco BARRETO, Vinicuis FOCHI, Alexandre M. AMORY, Fernando G. MORAES (PUCRS, Brazil)

12:20 - 14:00 Lunch

14:00 - 14:40 Invited Talk

Spin Transfer Torque Memories for On-chip Caches: Prospects and Perspectives

Kaushik Roy – Purdue University, USA
Chair: Yervant Zorian – Synopsys, USA

14:40 - 15:20 Special Session 2

Emerging Nanotechnologies

Organizer: Subhasish Mitra (Stanford University, USA)

Three-Independent-Gate Transistors: Opportunities in Digital, Analog and RF Applications
Pierre-Emmanuel GAILLARDON (University of Utah, USA)

Processor-Level Implications of Emerging Technologies
Robert AITKEN (ARM, USA)

15:20 - 16:30 PhD & Master Contests

TTTC's McCluskey Best 2016 Latin American PhD Thesis Contest

Master Thesis Contest

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16:30 - 16:50 Coffee Break

16:50 - 17:50 Session 10

Verification and System Level Testing

Chair: Jacob Abraham – University of Texas, USA

A SystemC-based Platform for Assertion-based Verification and Mutation Analysis in Systems Biology
Nicola BOMBIERI (University of Verona, Italy), Rosalba GIUGNO (University of Catania, Italy), Franco FUMMI, Carlo LAUDANNA, Rosario DISTEFANO, Daniele COATI, Michela MIRENDA (University of Verona, Italy)

Infrastructure for Formal and Dynamic Verification of Peripheral Programming Model
Walter ENCINAS, Francisco ARAUJO, Harney ABRAHIM (Freescale Semicondutores, Brazil)

System-Level Diagnosis for WSN: A Heuristic
Mauricio BARROS, Andrea WEBER (UFPR, Brazil)

17:50 - 18:30 Closing Remarks

Award Ceremony for the PhD and Master Thesis Contests

Saturday, 9th April 2016

09:00 - 12:00 TTEP 1

Hierarchical Test for Today's SOC and IoT

Yervant Zorian - Synopsys, USA

14:00 - 17:00 TTEP 2

Combining Structural and Functional Test Approaches across System Levels

Artur Jutman - Testonica Lab, Estonia
Hans-Joachim Wunderlich - University of Stuttgart, Germany
Matteo Sonza Reorda - Politecnico di Torino, Italy

General Chairs:
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Past General Chair:
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Program Chairs:
Matteo Sonza Reorda – Politecnico di Torino, Italy
Tiago Balen – UFRGS, Brazil

Special Session Chair:
Vishwani Agrawal – Auburn University, USA

Panel Chairs:
Raoul Velazco – TIMA Laboratories, France
Fernanda Kastensmidt – UFRGS, Brazil

Publication Chairs:
Maksim Jenihhin – Tallinn University of Technology, Estonia

Publicity Chairs:
Giorgio Di Natale – LIRMM, France
Ricardo Reis – UFRGS, Brazil
Adit Singh - Auburn University, USA
Xiaoqing Wen - KYUTECH, Japan

TTTC's E. J. McCluskey Best 2016 Latin American PhD Thesis Contest Organizer:
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Raoul Velazco – TIMA Laboratories, France
Yervant Zorian – Synopsys, USA

Fault Simulation in Radiation-Hardened SOI CMOS VLSIs using Universal Compact MOSFET Model

Konstantin O. Petrosyants[1,2], Lev M. Sambursky[1,2], Igor A. Kharitonov[1], Boris G. Lvov[1]

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***Abstract*—The methodology of modeling and simulation of environmentally induced faults in radiation hardened SOI CMOS ICs is presented. For this purpose, the universal compact SPICE SOI MOSFET model with account for TID, dose rate and single event effects is used. First, the model parameters extraction procedure is described in more details taking into consideration radiation effects and peculiarities of novel radiation-hardened (RH) SOI MOS structures. The results of analog and digital SOI CMOS circuits simulation show the difference with experimental data not more than 10–20% for all types of radiation.**

Keywords—SOI CMOS circuits; fault modeling and simulation, radiation hardness; TID, dose rate, single events; compact SPICE models; novel RH SOI MOS structures; model parameter extraction.

I. INTRODUCTION

Silicon-on-Insulator (SOI) technology has over many years generated great interest for radiation-hardened integrated circuits (RH IC) applications [1]–[3]. SOI circuits are tolerant to radiation-induced latch-up and less prone to single-event upset (SEU) phenomena, in comparison to bulk technologies. However, SOI technologies show a total-dose vulnerability since most of radiation-induced defects are accumulated in the thick buried oxide layers of BOX and shallow-trench isolation (STI). Therefore, total-dose effects in SOI MOSFETs being under gamma and X-rays radiation have been of much interest.

RH ICs are fabricated by modified processes and contain CMOS transistors with novel structures to provide additional radiation tolerance, in comparison with standard CMOS circuits. For RH ICs so-called "Rad-Hard by Design" (RHBD) methodology is used.

Environmentally induced failures in CMOS VLSIs are generally caused by three types of effects: 1) MOSFET threshold voltage shift and leakage current increase due to total ionizing dose (TID), 2) photocurrents due to dose rate, 3) transient currents due to single events.

It was shown that failures in CMOS circuits could be determined and forecasted through SPICE simulation using compact device models taking into account radiation effects [4].

For this purpose, several compact SPICE SOI MOSFET models were developed taking into account TID, dose rate and single event effects [4]–[15]. In [5] compact model TDESim for submicron devices was proposed to account for radiation-induced sidewall static leakage currents in "bird's beak" LOCOS corners. Paper [6] introduced a compact model with account for single events and total dose effects on threshold voltage and mobility. The model does not account for buried oxide radiation-induced effects and the arising leakage currents. Paper [7] presented a macromodel with simple polynomial-based account for threshold voltage, mobility, and sidewall leakage currents with varying body contact voltage. Article [8] details a physics-based compact model with account for TID and aging effects in devices based on surface potential calculations. In [6], [9] a more accurate compact model for SEU simulation including deposited charge recombination and charge decreasing by transistor current was proposed. However, in this model the major parameter (current gain) of parasitic bipolar transistor influence on the induced current was not written in detail. Articles [10]–[13] present SOI/SOS-MIEM and BSIMSOI-RAD compact models for SOI/SOS MOSFETs with account for various radiation effects, however parameter extraction procedure was not developed sufficiently. SPICE modeling of pulsed ionizing radiation influence was addressed in [14], [15]. The model [14] accounts for the difference in drain and source photocurrents, forward biasing of drain junction. [15] presents a method to characterize bipolar amplification.

However, summarizing the results presented in these works, we are forced to consider that the model parameters extraction procedure was not carried out completely, especially for novel rad-hard SOI CMOS transistor structures. This fact creates numerous problems for RH CMOS ICs design.

In the presented work, authors have solved this problem. The most advanced for today compact SPICE model for rad-hard SOI MOSFETs taking into account TID, dose rate, and single event effects [16] was considered. The conventional methodology of model parameters extraction understandable for device and circuit designers was proposed. The examples of fault simulation of analog and digital RH SOI/SOS CMOS circuits demonstrate the efficiency of using the proposed universal model in rad-hard IC design strategy.

This work was supported in part by the National Research University–Higher School of Economics, Academic Fund Program in 2015, grant No. 15-01-0165, and Russian Foundation for Basic Research, grant No.14-29-09145.

II. Rad-Hard Device Structures

The radiation-hard SOI MOS transistor structures (H- or O- or R-type) are essentially needed in addition to common linear (called F- or I-type) (see Fig. 1) devices to exclude or suppress the radiation-induced effects of trapped oxide charge and excess charge collection to gain the device radiation hardness. In these structures, lateral radiation-induced leakage currents are effectively suppressed or their active silicon areas have no lateral sides at all.

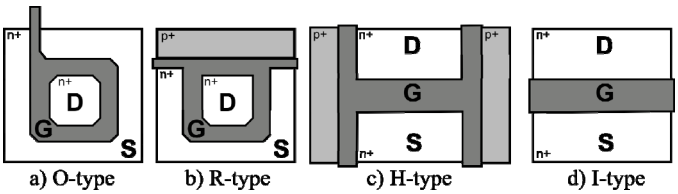


Fig. 1. Layout of different types of radiation hardened MOSFETs (O-, R- and H-types) used to suppress leakage currents vs. the linear type (I-type)

III. Rad-Hard SPICE SOI MOSFET Macromodel

The last version of the most advanced compact SPICE model for SOI MOSFET with account for total ionizing dose induced effects (TID), pulsed radiation effects, single events is presented in Fig. 2 [16]. The equivalent circuit of the model consists of two parts:

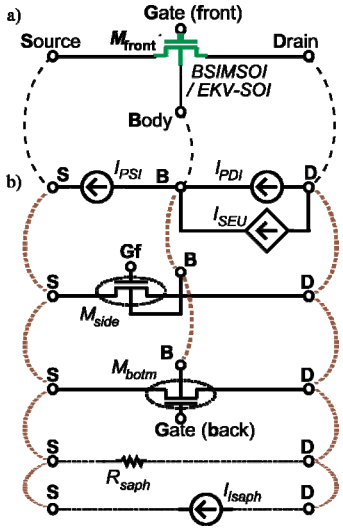


Fig. 2. Equivalent circuits of the BSIMSOI-RAD and EKV-RAD macromodels for SOI/SOS MOSFET: *a*—core front MOSFET M_{front} with radiation dependent parameters; *b*—subcircuit for radiation-induced static and dynamic leakage currents

1) Core model based on standard BSIMSOI [17] or EKV-SOI [13] platforms for submicron main transistor M_{front} (front Si–SiO_2 interface) with parameters dependent on TID. The type of model platform is selected by designer,

2) Additional subcircuits taking into account radiation-induced effects. Parasitic transistors M_{botm} and M_{side} are used for the backgate and sidewall leakage currents in MOSFET structure (see Fig. 3). Model parameters of the main M_{front} and parasitic transistors M_{side} and M_{botm} standing for threshold voltage V_T, mobility μ_{eff} and subthreshold slope S are radiation-dependent and are described with mathematical equations. Current sources I_{PSI}, I_{PDI} represent the currents induced by pulsed irradiation; current source I_{SEU} represents the current induced by ion strike; I_{lsaph} and R_{saph} represent steady-state radiation-induced leakage current along the insulating sapphire substrate and sub-surface transient ionizing radiation-induced leakage current, correspondingly, for the case of SOS MOSFETs.

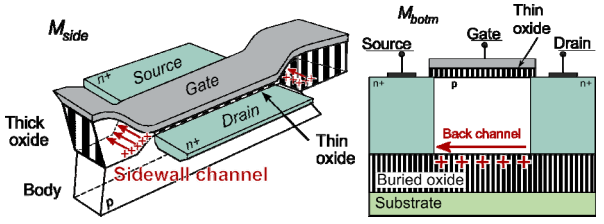


Fig. 3. Location of parasitic channels for leakage currents in SOI MOSFET structure: sidewall (STI) (a) and back (BOX) (b) channels

1) Total-dose effects:

In BSIMSOI, radiation-dependent parameters are parameters for threshold voltage (*VTH0* with factors *K1*, *K2* etc.), mobility (*U0* with factors *UA*, *UB* etc.), and subthreshold slope (*CIT* and *VOFF*); in EKV-SOI, these are *VTO, GAMMA, KP,* and *E0*; in parasitic transistors: *VTO, THETA, UO, NFS*. The dependence of the named parameters on total dose D is expressed in the form with saturation plateau for high doses:

$$a_1 \cdot (1 - \exp[-a_2 \cdot D]), \qquad (1)$$

or in the form of a polynomial. In (1) a_1, a_2 are fitting factors related to ionization dose and electrical bias during irradiation. Fitting factors in these expressions constitute the set of static radiation parameters of the macromodel.

2) Single events

The proposed single events modeling approach is based on [9]. The schematic representation of the proposed model for SEU is shown in Fig. 4,*b*.

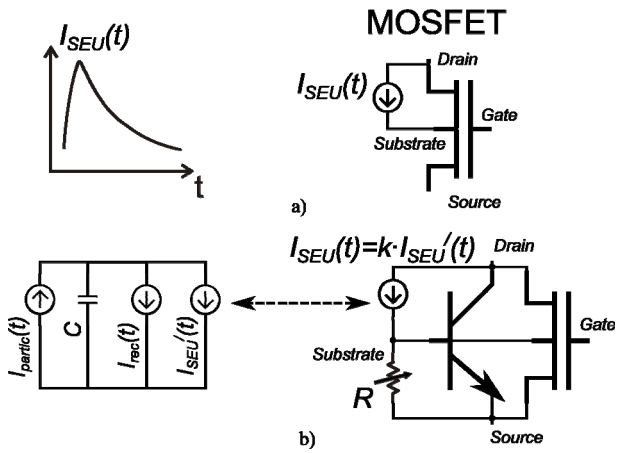


Fig. 4. SPICE-modeling of SEU in SOI MOSFET: a) simple model with double-exponential current source (a), improved model (b) with subcircuit connected to MOSFET

Independent current source I_{partic} represents the basic time-current profile of the transient radiation-induced current, e. g. a double exponent. The capacitor C is used to ensure charge conservation; its voltage is proportional to the charge that has not been dissipated by the two dependent source branches. The I_{SEU} and $I_{SEU}/$ dependent current sources represent the radiation-induced current at the p-n-junction. The current through I_{SEU} is proportional to the voltage across C and is a function of the voltage across the internal transistor junction. The I_{rec} dependent current source accounts for recombination currents.

In comparison with the predecessor model [9] (Fig. 4,*a*), the proposed model accounts for the known dependence of parasitic bipolar transistor gain on track location in SOI/SOS

MOSFET structure: no amplification for track located at drain region and amplification value much greater than 1 for track located at gate region.

BSIMSOI model already contains a parasitic bipolar transistor of SOI MOSFET structure. So to account for the known dependence of amplification gain on track location in SOI/SOS MOSFET structure, an additional resistor *R* was introduced.

3) Dose Rate Effects

Dose rate modeling follows the approach of [14] with current sources I_{PDI}, I_{PSI} (see Fig. 5), a diode to account for forward biasing the drain junction, and a parasitic BJT. Given that the analyzed MOFETs are situated on the insulating substrate and have thin active layer, transient photocurrents include only the prompt components and are described by the well-known equations [18]:

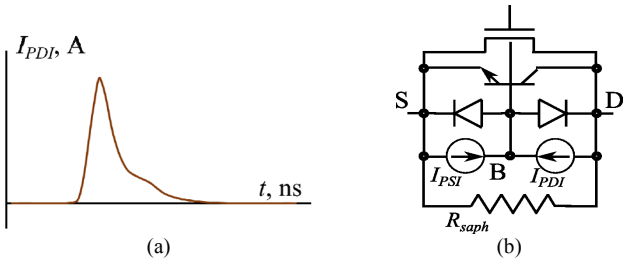
$$I_{PDI} = qg_0\gamma(t)\cdot V_{col}(V_{DS}) \qquad (2)$$

where q is the elementary charge; g_0 is the generation rate in silicon = $4\cdot10^{13}$ (electron-hole pairs rad^{-1}cm^{-3}); $\gamma(t)$ is the dose rate (rad(Si)/s); $V_{col}(V_{DS})$ is the function describing the effective collection volume (cm^3) which is drain voltage V_{DS} dependent.

Moreover, R_{saph} resistor accounts for sapphire conductance during transient ionizing radiation pulse:

$$R_{saph}(t) = K_{saph}L\big/\big(Wd\gamma(t)\big), \qquad (3)$$

where K_{saph}=6.8 10^{-14} (Ohm cm rad/s); *L and W* are transistor gate length and width; *d* is thickness of conductive region of sapphire under transistor.



(a) (b)

Fig. 5. SPICE-modeling of dose rate effects: a) radiation pulse exemplary shape, b) subcircuit connected to MOSFET

IV. Macromodel Parameter Measurement and Extraction Strategy

A. Modified Procedure for MOSFET Characteristic Measurement

The modified electrical measurement procedure [19] is formed on top of the standard one that is launched several times during the whole process. The modification is necessary to separately characterize the parasitic components of the macromodel that replaces a standard SPICE model to account for radiation-induced leakage currents. Irradiated MOSFETs electrical characteristics data may come from real test structures measurements, or from device simulation with TCAD ([19] presents the corresponding dataflow within the specialized hardware-software system).

The parameter extraction procedure is automated with industry extraction tool IC-CAP, which simplifies data exchange and processing, lowers the human error probability. The input data are the sets of I-V and C-V curves of the standard SOI/SOS MOSFET structures at different values of total dose. These sets are transferred to IC-CAP using an in-house program interface.

The Standard Procedure. In the course of the standard measurement procedure, a number of standard electrical characteristic curves of a number of length- and width-varied MOSFET devices under test are measured under the control of IC-CAP and processed therein: "Id-Vg" and "Id-Vd" curves at various body voltages V_B; input and output curves for parasitic bipolar transistor

The Modified Procedure with an Account for Total Ionizing Dose. 1) The unirradiated front MOSFET model is fully measured with the standard procedure, parasitic MOSFETs being switched off.

2) A shortened (minimum, see below) set of electrical curves is measured on the devices under test after each of the scheduled radiation exposure levels the device has undergone. All the three interfaces (front, bottom, and sidewall) are activated sequentially with the help of special test structures, so that the radiation-induced leakage currents are separated:

- *R*- or an *O*-type ring transistor or *H*-type transistor with almost no lateral leakage, is used for separate measurement of I-V curves of the front MOSFET for different values of total dose at voltage $V_{Gb} < 0$ on the back gate, which excludes the effect of M_{botm}.
- The same structure type is used for separate measurement of I-V curves of the bottom parasitic MOSFET for several values of total dose at voltage $V_{Gf} < 0$ on the front gate, which excludes the effect of M_{front}.
- *F*- or *I*-type linear transistor or *A*-type transistor with both bottom and lateral leakage is used for separate measurement of I-V curves of the lateral parasitic MOSFET's at voltage $V_{Gb} < 0$ on the back gate to exclude the effect of M_{botm}.

For every single dose level, a shortened set of electrical curves is measured for the front, sidewall and bottom MOSFETs: "Id-Vg" and "Id-Vd" curves at a few drain voltages and fixed body voltage.

Automation of MOSFET Curve Measurement. Automation of curve measurement and data processing is highly desirable to reduce time of operation and human error. A measurement data acquisition and formatting suite was developed by tying up of IC-CAP and LabView tools with instrumentation. All the curve measurements of a single transistor are carried out without re-connection of the device under test, which further reduces risks of human error and device damage.

B. Strategy for SPICE Model Radiation Parameter Extraction

At the measurement stage, a set of characteristic curves is measured for every component of the macromodel. It is there-

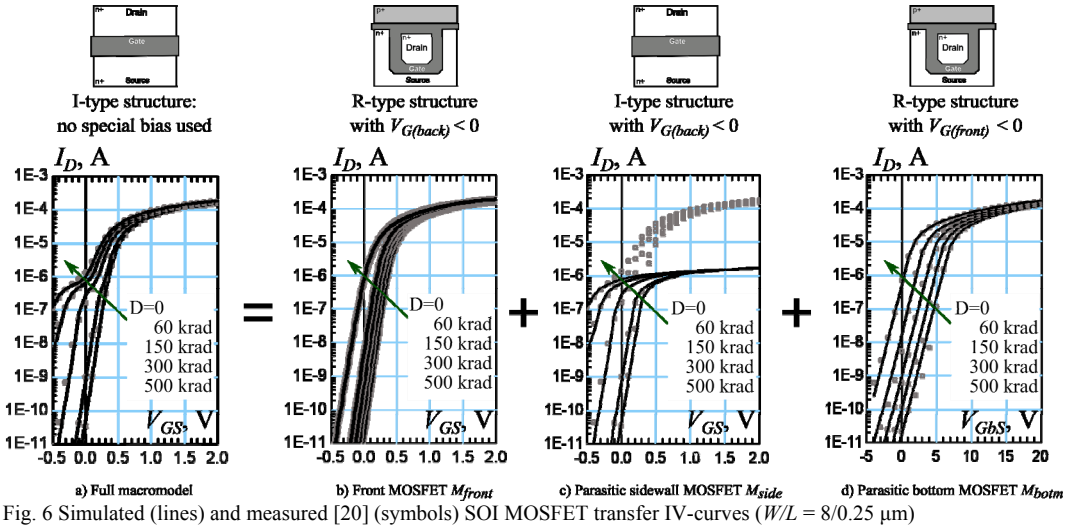


Fig. 6 Simulated (lines) and measured [20] (symbols) SOI MOSFET transfer IV-curves (W/L = 8/0.25 μm)

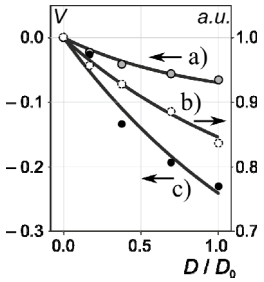


Fig. 7. Model parameters dependencies on dose for the main M_{front} transistor: ΔVOFF (a), U0(D)/U0(0) (b), ΔVTH0 (c)

fore possible to identify the model for each component separately, and then combine the resulting models into a single macromodel card.

Macromodel parameter extraction procedure with account for total dose effects is accomplished with the help of a modified workflow [17], [12] based on test structures measurement.

Modification of the extraction procedure is necessary given that for the irradiated devices: 1) *measurement results database* significantly grows in size and transforms; 2) the set of *test structures* enlarges; 3) *quantity of model parameters* increases; 4) the extraction procedure incorporates a new *step of approximation* of experimental dependencies of model parameters on dose to a known physical function.

The following strategy is developed:

1) The full set of macromodel parameters is at first extracted for the unirradiated device. The standard extraction flow inside IC-CAP sequentially invokes measurement data to identify the whole set of device model parameters group by group.

2) Among all the model parameters for MOSFET subcomponents a limited number of radiation-dependent parameters is selected: threshold voltage, mobility, subthreshold slope and their factors (depending on the selected models).

3) For each radiation dose D_i IC-CAP is used for extraction of the set of $V_T(D_i)$, μ(D_i), $S(D_i)$ etc. This procedure is repeated for all the doses D_i: i=1,n.

4) The sets of $V_T(D_i)$, μ(D_i), $S(D_i)$ etc. are approximated with analytical functions of the type: $a_1(1 - \exp[- a_2 \cdot D])$.

5) The determined functions are embedded into the MOSFET SPICE macromodel card that is further included into the SPICE model library.

Automation of the parameter extraction procedure with IC-CAP simplifies data exchange and processing, lowers the human error probability.

Duration of the parameter extraction procedure on the example of a set of 16 test transistors with different size and 6 doses of radiation for the case of BSIMSOI-RAD estimates to 166 minutes, while for EKV-RAD this figure is 123 minutes.

The extraction strategy is illustrated on the example of SOI MOSFET with gate dimensions W/L = 8/0.25 μm. Separate experimental characteristic curves for the main transistor M_{front} (Fig. 6,*b*) and parasitic bottom (Fig. 6,*d*), sidewall (Fig. 6,*c*) transistors were obtained [20]. The total SOI MOSFET current (Fig. 6,*a*) is the Kirchhoff sum of partial currents (Fig. 6,*b,c,d*). The set of macromodel parameters was determined by means of the described extraction strategy. The dependencies of parameters on dose D were approximated with analytical functions of type $a_1(1 - \exp[- a_2 \cdot D])$ (see Fig. 7). The error between measured and simulated I-V-characteristics is 10–15%.

V. Fault Simulation in RH SOI CMOS Circuits

Validation of the proposed model's capability to predict circuit failure if faced with various radiation effects is demonstrated on the examples of a set of digital and analog circuits.

A. Total-Dose Effects

TID causes the threshold voltage shift and leakage current increase in SOI/SOS MOSFETs. Both effects have significant impact upon analog and digital circuit operation.

For example, Fig. 8 presents measured and simulated at various values of total dose frequency response for a SOI CMOS OA (35 MOSFETs) fabricated by XFAB 1 μm technology. It is indicated that op-amp performance is degraded by TID effects, especially when the radiation dose is larger than 250 krad. The DC gain degradation is significantly large with a loss of 50 %. In Fig. 9 measured and simulated voltage transfer and supply current characteristics are shown for a SOS CMOS inverter. It was found that for total dose greater than 1 Mrad the failure occurs. Fig. 10 depicts simulated and measured delay time values for a SOS CMOS FDC flip-flop (48 MOSFETs). For this circuit the maximal delay time is established as 50 ns, so the maximal allowed total dose is about 450 krad.

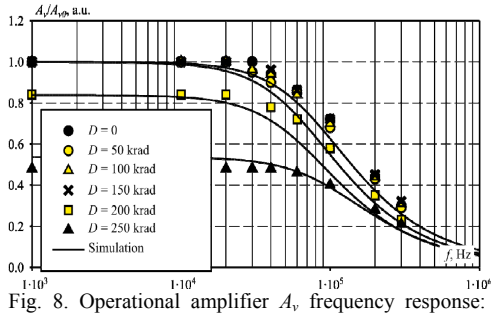


Fig. 8. Operational amplifier A_v frequency response: simulation (solid lines), experiment (points)

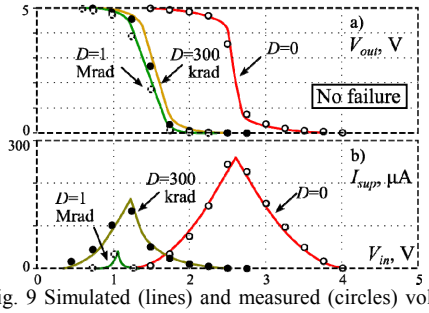


Fig. 9 Simulated (lines) and measured (circles) voltage transfer and supply current characteristics for a SOS CMOS inverter with L = 3 μm, t_{Si} = 0.6 μm

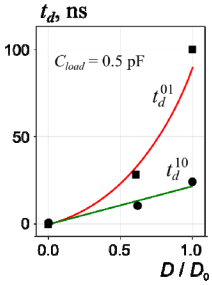


Fig. 10. SOS CMOS FDC flip-flop: measured (symbols) vs. simulated (lines) delay time with account for TID effects

In the presented examples, measurement and simulation were done by the authors; the simulation error is 10–15% for static and 15–20% for dynamic characteristics. Measurement data were obtained from Co-60 250 krad/h source.

B. Single Events

For the case of single event upsets (SEU), we firstly conducted circuit simulation of an ion strike on 6T CMOS memory cell (Fig. 11). MOSFET structure parameters were the following: W/L=1.4/0.5 μm, buried oxide thickness – 150 nm, active Si layer thickness – 190 nm, gate oxide thickness – 11.5 nm. Fig. 12 presents transient characteristics of the cell modeled for ion with different values of linear energy transfer (LET). It is seen that operation failed when ions had LET larger than 20 MeV·cm^2/mg.

Secondly, we investigated the effect of MOSFET body contact presence on failure level of the same cell. Transient characteristics were modeled for ion with *LET* = 0,216 pCl / μm (which is equivalent to Fe ion with 16 MeV energy), which impacts the transistor layout at an angle of 30 degrees to the surface. Fig. 13 presents transient characteristics of the cell modeled with two layout versions of MOSFETs: with and without a special contact to transistor body. I_D curve shows the impacted MOSFET (MPA) drain current; the moment of its pulse onset is the time of particle impact. In the case where there is no body contact, the circuit fails—both points A and B change their states, while in the case where the body contact is present, the circuit successfully operates—points A and B only experience glitches, but eventually return to the initial states. So, the additional contact to transistor body gains radiation hardness.

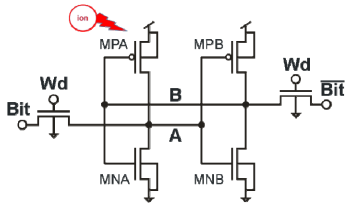


Fig. 11. 6T CMOS memory cell schematic representation for circuit fault simulation

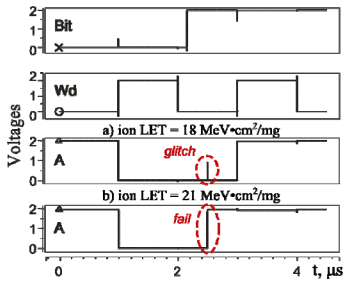


Fig. 12. Fault simulation of SEU in a 6T CMOS memory cell (Fig. 11) with different values of linear energy transfer (LET): operation succeeded (a), operation failed (b)

Thirdly, Fig. 14 shows simulation results for drain voltage and drain current of the MPA transistor in cell Fig. 11 after ion impact into the border between gate and drain regions. Mixed-mode TCAD-SPICE and two variants of SPICE simulation (ideal double exponential current source and the proposed model) are compared. It is seen that the simpler model grossly overestimates parasitic bipolar amplification in the impacted MOSFET, while the proposed model provides error less than 20% compared to TCAD-SPICE exemplar.

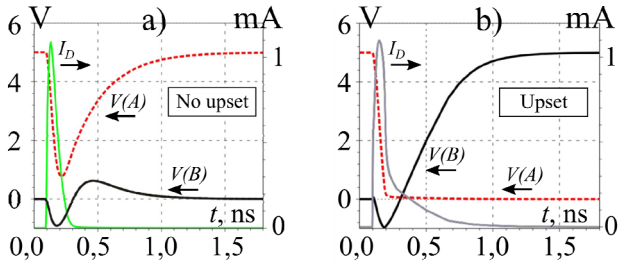


Fig. 13. Fault simulation of SEU in a 6T CMOS memory cell (Fig. 11) with (a) and without (b) a body contact in a transistor structure: operation succeeded (a), operation failed (b)

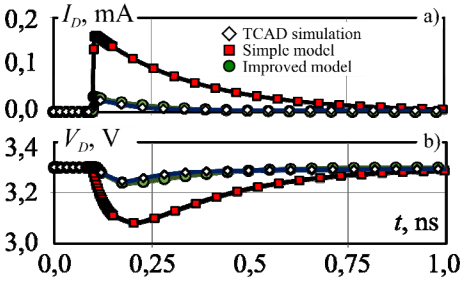


Fig. 14. Mixed-mode SPICE-TCAD simulation vs. SPICE-only simulation (simple and improved model) of SEU in a 6T CMOS memory cell (Fig. 11)

C. Dose Rate Effects

The validation of the model Fig. 5 was carried out on two examples of photocurrent simulation: for single SOS CMOS inverter fabricated by 2 μm SOS technology (in-house measurements) and for array of SOI MOSFETs fabricated by Honeywell 0.15 μm SOI technology [14].

Fig. 15 shows that SOS CMOS devices with thinner Silicon layer t_{Si} = 0.3 μm have smaller effective collection volume V_{col}

(see (2)) and as a result, they are more resistant to pulse irradiation. However, the pulse with dose rate $1 \cdot 10^{12}$ rad/s does not cause failure in an SOS CMOS inverter with two values of Silicon layer thickness of 0.6 and 0.3 μm.

Fig. 16 presents radiation-induced leakage currents data per a single transistor for an array of 80,000 n-channel SOI MOSFETs with W/L = 0.4/0.15 μm. The radiation pulse had both rising and falling edges of 10 ns and width of 13 ns with varying dose rate. Negligible parasitic bipolar effect was found. The simulation results are in good agreement with experimental data [14].

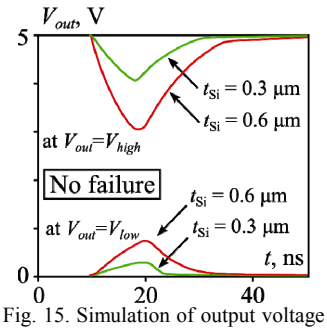


Fig. 15. Simulation of output voltage transients after pulsed irradiation for SOS CMOS inverter with L = 2 μm, t_{Si} = 0.3 and 0.6 μm

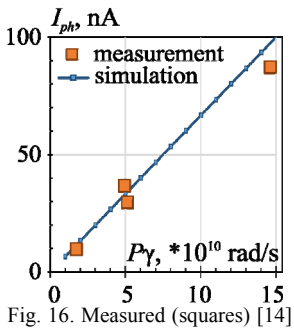


Fig. 16. Measured (squares) [14] and simulated (lines) pulsed irradiation induced SOI MOSFET photo current per one transistor

VI. Conclusions

Fault modeling and simulation of rad-hard SOI/SOS CMOS ICs using SPICE compact SOI/SOS MOSFET model is an effective design technique for improving IC radiation hardness, cutting down the number of expensive fabrication runs. The advanced universal compact SOI/SOS MOSFET model taking into account TID, dose rate, single event effects and peculiarities of novel rad-hard SOI MOS structures was used for circuit simulation. The conventional methodology of model parameters extraction from experimental data understandable for device and circuit designers was proposed.

Modeling error of 10–15 % for static and 15–20% for dynamic characteristics of SOI MOSFETs was achieved using the developed SPICE parameter extraction procedure.

The model was implemented in commercial circuit simulators HSpice, Spectre, Eldo and others and extensively applied to simulation of analog, digital, and mixed-signal rad-hard SOI/SOS CMOS ICs.

The examples of radiation induced parameter degradation and fault simulation of analog and digital rad-hard SOI/SOS CMOS ICs were presented to demonstrate the efficiency of using RH BD strategy.

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