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Electro-thermal Design of Smart Power Devices and Integrated Circuits.

Konstantin O. Petrosyants*[1,2,a], Igor A. Kharitonov[1,2,b] and Nikita I. Ryabov[1,c]

[1]Moscow Institute of Electronics and Mathematics of National Research University

"Higher School of Economics", 20 Myasnitskaya Ulitsa, Moscow, 101000, Russia

[2]Science and Research Institute for Microelectronics and Instrumentation,
B. Trekhsvyatitelsky per., Moscow, 109028, Russia

[a]eande@miem.edu.ru, [b]ikharitonov@hse.ru, [c]nryabov@hse.ru

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Abstract. An efficient methodology of electro-thermal design of smart power semiconductor devices and ICs, based on the combined use of SPICE circuit analysis tool and software tools for 2D/3D thermal simulation of IC chip construction, is presented. The features of low, medium and high power elements, temperature sensors, IC chips simulation are considered.

Introduction

Smart power ICs and modules are the perspective components for industrial automation, robotics, automotive and avionics, marine and space navigation, telecommunications, computer peripherals, communications equipment, electronic data processing etc. As it is known [1], the following main features are inherent to them: 1) combination of powerful output transistors or control circuits with low and middle power circuits for control, diagnostics and protection, as well as logic circuits, A/D and D/A converters, memory cells, etc. on IC chip; 2) operation at high current levels (more than 1 A) and voltages (up to 1000 V and above), under strong heating conditions (more than 150 °C) for output stages, in conjunction with the high requirements to linearity and sensitivity for sensor and analog components, and 3) the possibility to work with inductive load (motor, generator, relays windings, etc.) in external environment of high temperature, vibration, environmental pollution, etc.

The electric power in such ICs can be tens or hundreds of Watts. To dissipate such power the output devices/stages can occupy from 30 to 70% of the total chip area. Obviously, the proper functioning of such ICs is impossible without their layout optimization, strict operating temperatures control and the use of thermal protection circuits [1].

As a consequence, one of the most important stages of "smart" power ICs and modules design is their electro-thermal design, that allows to choose optimal electrical and thermal modes of operation for IC elements, to develop and design the circuit layout, providing first, the lowest possible heating and thermal interaction between elements on the chip and the best conditions for the heat flow to the environment through IC case and, secondly, the minimum thermal chip gradients that do not result in the chip mechanical deformation or even its crack.

Therefore to effectively design smart power ICs one has to solve the following tasks:
– calculation of temperature distribution along the chip surface,
– generation of the electro-thermal models for elements and electro-thermal simulation of the chip,
– account for thermal interaction between elements,
– finding optimal construction and placement of temperature sensors.

The subsystem for electro-thermal design of smart power chip/elements

With the aim of solving the problems described above the subsystem for electro-thermal design of smart power chip/elements has been developed and used by us and our colleagues for real projects. Electro-thermal design has been realized by the subsystem using two main kinds of software packages: circuit analysis tool (SPICE, Eldo from Mentor Graphics, Spectre from Cadence have

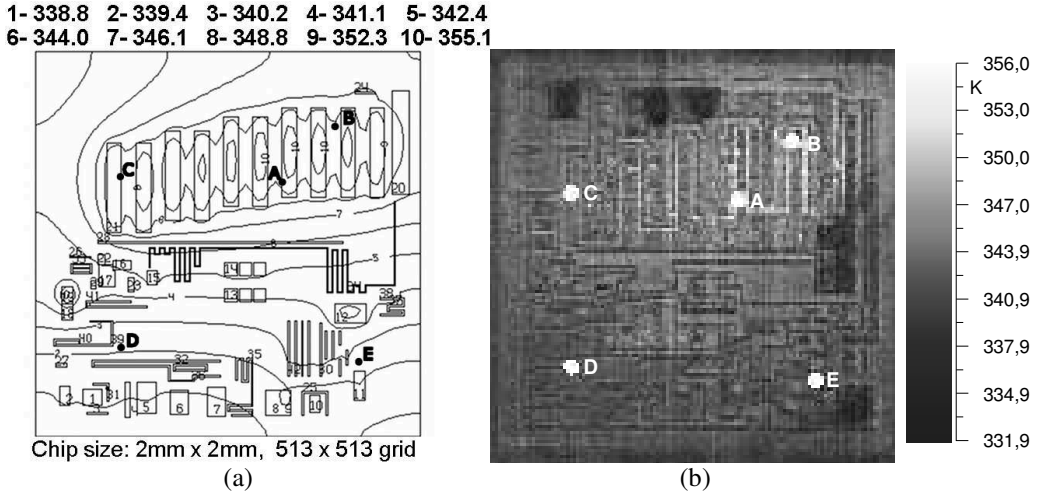
been used) and our own tools for 2D or 3D simulation of thermal fields in IC chips. The simulation tools of the subsystem have been combined with the standard layout design tools [2].

The electro-thermal design procedure was as follows.

The 3D simulation software tools [2] were used at the *first step* of electro-thermal simulation procedure to simulate the temperature distribution along the chip surface and cross section and then to calculate the matrices with thermal resistance and capacitance for necessary chip elements. At the *second step* the circuit simulation tools (SPICE, Eldo, Spectre Tools) were used for electro-thermal simulation of the IC with electro-thermal SPICE models and thermal resistances and capacitances calculated earlier. Such approach provided much faster simulation in comparison with the approach where 2D/3D thermal simulator is used together with SPICE simulator at each iteration of electro-thermal simulation process.

IC chip thermal simulation software tool.

The Overheat software tool has been developed to solve the 3D heat transfer equation for IC chip structure using Fast Fourier Transformation [2]. The results of simulation are temperature distribution along the chip surface and thermal resistances and capacitances for chip elements. As an example Fig. 1 presents the simulated temperature distribution along the surface of integrated voltage regulator 142EN9 chip (V_{IN}=40 V, V_{OUT}=27 V, P=7 W) produced with bipolar technology. The measured temperature distribution along the IC chip surface (see Fig. 2(b)) was obtained with FLIR A-40 IR camera. A good agreement between the measured and simulated 2D temperature distributions can be seen.



(a) (b)

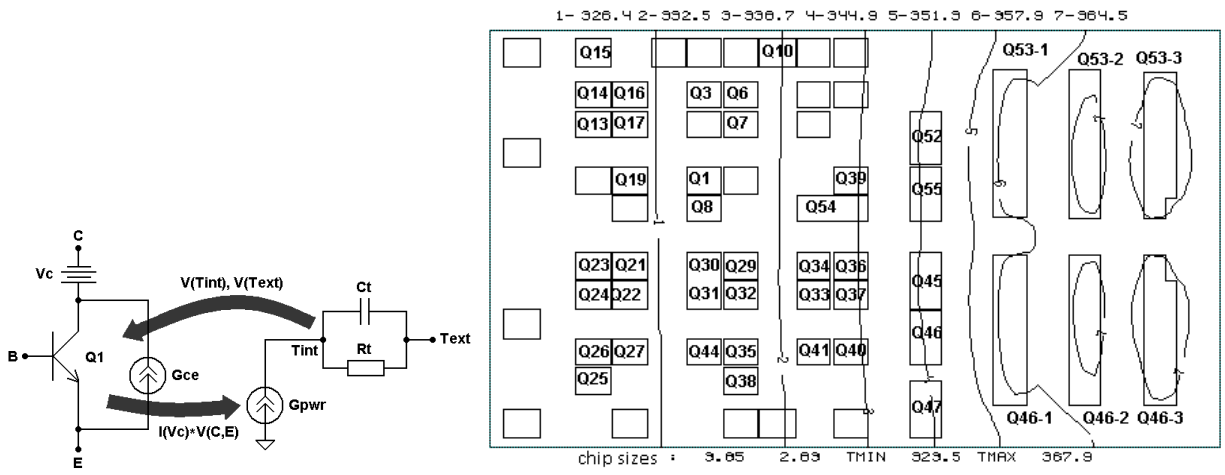
Figure 1. The simulated with Overheat (a) and measured with Flir A40 IR camera (b) temperature distribution along the voltage regulator 142EN9 chip surface .

Electro- thermal SPICE models of IC elements.

High power transistors operating at high current and voltage levels and high temperatures impose specific requirements for their SPICE models. Besides the physical effects in low-and middle-power elements (both BJT and MOSFET) the high power devices exhibit additional effects: self-heating and thermal avalanche breakdown, semiconductor regions resistance modulation and others whose influence must be considered and simulated in IC design stage. There are many published papers on power transistor SPICE models, considering various aspects of their modelling but not all the major problems have been solved. In course of our work we have developed a SPICE model library of smart power IC elements [3]: BJTs, MOSFETs and others. The library can be used with a different version of SPICE simulator, including Eldo (Mentor Graphics), Spectre/Ultrasim (Cadence). These models are electro-thermal and account for effects of temperature on transistor parameters and terminal currents (Fig. 2 (a)).

Smart power IC chip electro-thermal simulation

The results of SPICE electro-thermal simulation of 4.5 Watt operational amplifier manufactured with analog IC bipolar technology are illustrated in Fig. 2 (b) and Table 1. Thermal resistances and capacitances for power transistors have been calculated with the Overheat software tool. Fig. 3 presents temperature distribution along the chip surface and it is seen that the maximum temperature is observed in the three-piece output power transistors Q46, Q53 and it reaches 70 °C. These transistors heated elements adjacent to them and changed their electric mode. Table 2 presents comparison between the current, power and temperature figures of Op Amp IC elements (see Fig. 2(b)) simulated with the conventional SPICE model and using electro-thermal simulation with models of Fig. 2 (a) and thermal network parameters calculated with Overheat. The difference between the conventional and electro-thermal SPICE simulation results is clear.



(a) (b)

Figure 2. Electro-thermal SPICE model for BJT (a) and Overheat tool simulated temperature distribution along the Op Amp IC chip surface (b).

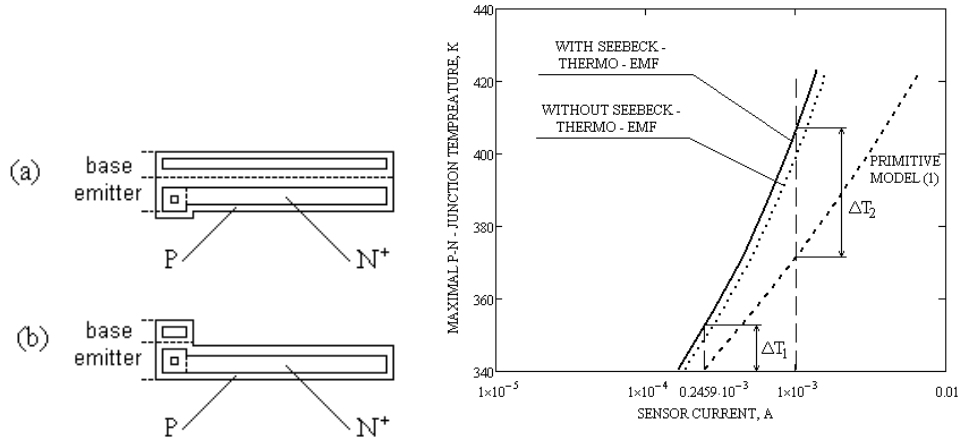
Table 1. Comparison between the current, power and temperature of Op Amp IC elements (see Fig. 2 (b)) simulated with the conventional SPICE model (left part) and using electro-thermal simulation with models (Fig. 2 (a)) (right part).

Transistor	Conventional SPICE simulated (Rload=85Ohm; Tcase=300K)			Electro-thermal SPICE simulated (Rload=85Ohm; Tcase=300K)		
	Collector current, A	Element power, W	Element temperature, K	Collector current, A	Element power, W	Element temperature, K
Q52	$6.5\ 10^{-4}$	$1.24\ 10^{-2}$	300	$1.62\ 10^{-3}$	$4.21\ 10^{-2}$	345
Q45	$6.4\ 10^{-4}$	$1.24\ 10^{-2}$	300	$1.66\ 10^{-3}$	$4.32\ 10^{-2}$	347
Q53	$1.37\ 10^{-2}$	0.274	300	0.145	1.75	369.3
Q46	$1.27\ 10^{-2}$	0.254	300	0.148	1.8	370

Design and simulation of temperature sensors integrated with power transistors.

Reliable operation of smart power IC elements is impossible without strict control of their operating temperatures and without creation of thermal protection circuits. Small-size low-current BJTs and MOSFETs are suitable as temperature sensors. BJTs and diodes have essential advantages over MOS transistors in terms of sensitivity and stability for a wide range of temperatures. For the stripped sensors temperature of the most heated power BJT is irregularly distributed along the sensor stripe. As it is known, the temperature gradient along the sensor generates Seebeck thermo-EMF [4] which influences the sensor output signal. So the choice of sensor location, its size and layout, as well as working electric modes should have been done using electro-thermal simulation. The Overheat software tool has been modified to account for the Seebeck thermo-EMF effect. The simulated dependences of maximal temperature of emitter sensor p-n–junction vs. sensor current for stripped sensor Fig. 3 (a, b) is shown in Fig. 3 (b). For example, for dissipated power P=3.7 W the sensor current is I_E=0.25 mA and maximal p-n – junction temperature is T_{MAX}=356 K; for P=15 W the corresponding values are I_E=1.0 mA and T_{MAX}=407 K. If the “primitive” model (the model

without account for both the voltage drop along the sensor strip and Seebeck effect) is used, the corresponding values of T_{MAX} for the same values of current are significantly lower: 340 K and 372K respectively. So the temperature measurement errors are 16 K and 35 K. It is too much for a power IC, especially for voltage regulators and power amplifiers.



(c)

Figure 3 Temperature sensors layouts: (a) - base contact is a stripe along emitter, (b) - base contact is a little area at the end of the region; (c) - simulated maximal sensor junction temperature vs sensor current for stripped sensor (a) with (solid line) and without (dotted line) Seebeck effect account.

Summary

The presented methodology, developed and modified software tools, SPICE models for components, IR measuring system showed their efficiency for smart power IC and device design.

Importance and methods to account for electro-thermal effects in smart power IC design process were demonstrated.

It was shown that parasitic effects of sensor current displacement and thermo-EMF generation resulting from temperature gradients had to be taken into account for correct temperature sensor design for power IC elements.

A good agreement between the simulated and IR-camera measured temperature distributions along smart power IC chip surfaces was achieved.

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Corresponding Author

Konstantin O. Petrosyants, eande@miem.edu.ru; kpetrosyants@hse.ru, 007-499-2355042

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