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Quasi – 3D Electrical and Thermal Modeling of Microelectronic Semiconductor Devices

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Abstract. New quasi – 3D numerical model for electrical and thermal analysis of microelectronic semiconductor devices is presented. The general 3D heat transfer and electrical field problems are correctly transformed to the set of 2D equations for temperature and electrical potential distributions in different layers of the device. The complexity and CPU time of the electro-thermal analysis are many times reduced. The results of different devices electro-thermal modeling for different types of semiconductor devices and ICs are presented.

Introduction

The constructions of most microelectronic semiconductor devices and integrated circuits (ICs) can be represented as 3D multilayer structures with different electrical and thermal conductivities. On the top of semiconductor chip the metallic contacts and interconnections are placed. The bottom surface of the chip is attached to the package through the adhesive layers (see Fig. 1).

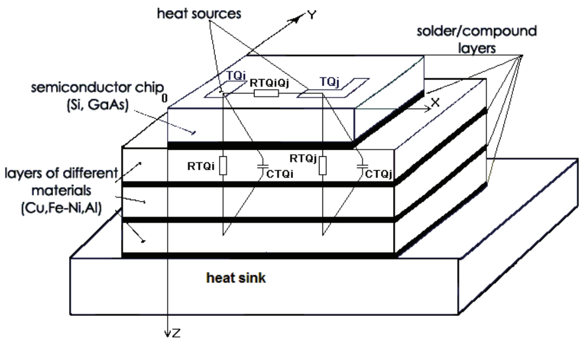


Figure 1. Integrated circuit package structure.

The steady-state electro-thermal conditions of semiconductor devices are described by the coupled pair of 3D differential equations:

1) equation for electrical potential distribution $U(x,y,z)$:

$$\frac{\partial}{\partial x}\left[\sigma\frac{\partial U}{\partial x}\right]+\frac{\partial}{\partial y}\left[\sigma\frac{\partial U}{\partial y}\right]+\frac{\partial}{\partial z}\left[\sigma\frac{\partial U}{\partial z}\right]=j\left(x,y,z,T,U\right), \quad (1)$$

where: σ, j – electrical conductivity and current density are dependent on the space variables (x,y,z);

2) equation for temperature distribution $T(x,y,z)$:

$$\frac{\partial}{\partial x}\left[\lambda\frac{\partial T}{\partial x}\right]+\frac{\partial}{\partial y}\left[\lambda\frac{\partial T}{\partial y}\right]+\frac{\partial}{\partial z}\left[\lambda\frac{\partial T}{\partial z}\right]=P\left(j,U,T\right), \quad (2)$$

where: $P(j,U,T)$ – electrical power distribution, $\lambda(x,y,z,T)$ – thermal conductivity.

For typical semiconductor devices and integrated circuits the function $j(U,T)$ and $P(U,T)$ in right-sides of (Eq. 1)-(Eq. 2) are non-linear functions of potential $U(x,y,z)$ and temperature $T(x,y,z)$, so no analytical solution can be used and consequently a numerical technique must be used to solve (Eq. 1)-(Eq. 2). The finite-difference technique has been used in the following analysis with respect to the different geometries that require simulation. Different boundary conditions are set on the top, bottom and out sides of the device and on the surfaces between internal layers in the structure Fig. 1.

In this paper several examples of (Eq. 1)-(Eq. 2) numerical solutions for different semiconductor devices are presented. To simplify the solution problems and minimize the SPU time the quasi-3D approach is used.

Quasi – 3D Approach Formulation

The traditional way to solve the problem (Eq. 1)-(Eq. 2) is using the universal 3D simulators: ANSYS [1], COSMOS [2], Flotherm [3], MSC/PATRAN [4], Sentaurus [5] etc. The advantages of this approach are its universality, adequacy and accuracy. But it has the serious limitations in practical application – very high computational cost and complexity of data processing.

So the quasi-3D approach is used to simplify the fully 3D solution problem (Eq. 1)-(Eq. 2) and minimize the SPU-time. This approach is based on the fact that for most microelectronic semiconductor devices and elements of monolithic and hybrid integrated circuits the geometrical sizes of devices l_x, l_y in horizontal place xy (see Fig. 1) are 10 – 100 times more, then their sizes in vertical direction z: $l_x, l_y > l_z$.

Because the layer thicknesses Δz_i of different materials in construction Fig. 1 are small ($\Delta z_i << l_x, l_y$), we can reasonably assume that in each point (x_i,y_j) the electrical potential $U(x_i,y_j,z)$ and temperature $T(x_i,y_j,z)$ in (Eq. 1)-(Eq. 2) are the linear functions of vertical coordinate z.

Then the fully 3D problem (Eq. 1)-(Eq. 2) is reduced to the set of 2D equations for different constructive layers:

$$\frac{\partial}{\partial x}\left[\sigma_\xi \frac{\partial U}{\partial x}\right]+\frac{\partial}{\partial y}\left[\sigma_\xi \frac{\partial U}{\partial y}\right]+\sigma_\xi \frac{U_\xi(x,y)-U_{\xi-1}(x,y)}{\Delta z_\xi}=j_\xi\left(x,y,T_\xi,U_\xi\right), \tag{3}$$

$$\frac{\partial}{\partial x}\left[\lambda_\xi \frac{\partial T}{\partial x}\right]+\frac{\partial}{\partial y}\left[\lambda_\xi \frac{\partial T}{\partial y}\right]+\lambda_\xi \frac{T_\xi(x,y)-T_{\xi-1}(x,y)}{\Delta z_\xi}=P_\xi\left(x,y,U_\xi,T_\xi\right), \tag{4}$$

where: $\xi=1,\ldots,K$ – number of the layer.

It is possible to use the numerical methods for the solution of the equations (Eq. 3)-(Eq. 4) and reduce the computational time considerably.

The vertical sizes of semiconductor IC, their elements and discrete transistors are close to layout sizes the described approach to them isn't applied. As the IC elements are located on the top surface of the chip and thickness of their active areas much less than thickness of the chip, in this case application of analytical methods for the solution of 3D thermal conductivity equation (Eq. 2) possible.

Thermal Fields Modeling in Semiconductor Integrated Circuits

The Mathematical Model of Semiconductor Integrated Circuits

It is the three-dimensional heat conduction equation (see Fig. 1):

$$\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}=0\,, \tag{5}$$

with the boundary conditions:

on the top of chip:

$$\lambda_1 \frac{\partial T}{\partial z}\bigg|_{z=0} = -P(x,y) + \alpha(T - T_{AMB}), \quad P(x,y) = \begin{cases} P_{EL} \big/ S_{EL} & (x,y) \in S_{EL} \\ 0 & (x,y) \notin S_{EL} \end{cases}, \tag{6}$$

on the boundaries of the different layers:

$$\lambda_i \frac{\partial T}{\partial z}\bigg|_{z=z_i-0} = \lambda_{i+1} \frac{\partial T}{\partial z}\bigg|_{z=z_i+0}, \quad T(x,y,z_i-0) = T(x,y,z_i+0), \tag{7}$$

on the package bottom the temperature is constant, but it is not equal to ambient temperature:

$$T(x,y,z_n) = T_{PACK} = \text{const}, \tag{8}$$

there is no heat exchange on the lateral surfaces of the chip:

$$\frac{\partial}{\partial x}\left[\lambda_\xi \frac{\partial T}{\partial x}\right] + \frac{\partial}{\partial y}\left[\lambda_\xi \frac{\partial T}{\partial y}\right] + \lambda_\xi \frac{T_\xi(x,y) - T_{\xi-1}(x,y)}{\Delta z_\xi} = P_\xi\left(x,y,U_\xi,T_\xi\right) \tag{9}$$

In (Eq. 5)-(Eq. 9) we use following notations: T - absolute temperature (K), P_{EL} - power of element (W), S_{EL} - area of element (mm2), λ_i - coefficients of thermal conductivity of layers (W/mm·K), T_{PACK} - temperature of package (K), T_{AMB} - the ambient temperature (K), α - coefficient of convective heat exchange (W/mm2·K), x_c, y_c - the chip sizes on layout plane (mm), z_i - the layer co-ordinates.

Numerical Method

For solving of the three-dimensional heat conduction equation (Eq. 5) with the boundary conditions (Eq. 6)-(Eq. 9) we use the separation of variables method with the discrete Fourier transformation and fast Fourier transformation algorithms (FFT) [6]. This solution has the form:

$$T_{i,j} = F^{-1}(F(P_{i,j}) \cdot \Theta_{k,l,1}), \quad i = 0,1,...,M_x, \quad j = 0,1,...M_y, \tag{10}$$

where: $T_{i,j}$ - the temperature of top of the chip in the difference network nodes; $P_{i,j}$ - power density in the difference network nodes; $F(\cdot)$, $F^{-1}(\cdot)$:

$$\begin{aligned} \tilde{f}_{k,l} &= F(f_{i,j}) = \frac{2}{\sqrt{M_x M_y}} \sum_{i=0}^{M_x}\sum_{j=0}^{M_y} f_{i,j} \cos\frac{k\pi i}{M_x}\cos\frac{l\pi j}{M_y}, \\ f_{i,j} &= F^{-1}(\tilde{f}_{k,l}) = \frac{2}{\sqrt{M_x M_y}} \sum_{k=0}^{M_x}\sum_{l=0}^{M_y} \tilde{f}_{k,l} \cos\frac{k\pi i}{M_x}\cos\frac{l\pi j}{M_y}, \end{aligned}, \tag{11}$$

- right and inverse discrete Fourier transformations, respectively; factors $\Theta_{k,l,1}$, k=0,...,M_x, l=0,...,M_y are solved from the boundary conditions (Eq. 6)-(Eq. 9), using the following recurrent formulas:

$$\Theta_{k,l,m} = \frac{\Psi_{k,l,m} + th(\sqrt{\mu_{k,l}}(z_{m+1} - z_m))}{1 + \Psi_{k,l,m} th(\sqrt{\mu_{k,l}}(z_{m+1} - z_m))}, \quad \frac{1}{\lambda_{m+1}}\Theta_{k,l,m+1} = \frac{1}{\lambda_m}\Psi_{k,l,m}, \quad \Psi_{k,l,n} = \frac{\sqrt{\mu_{k,l}}\lambda_n}{\alpha},, \tag{12}$$

i,j - indices of the difference network nodes; k,l - numbers of Fourier coefficients of network functions; M_x, M_y - quantity of the difference network nodes; m=n,...,1 - number of layer of structure; n - quantity of layers; $\mu_{k,l}$ - eigenvalues of the difference analogue of the 2D Laplacian; h_x, h_y - the difference network steps.

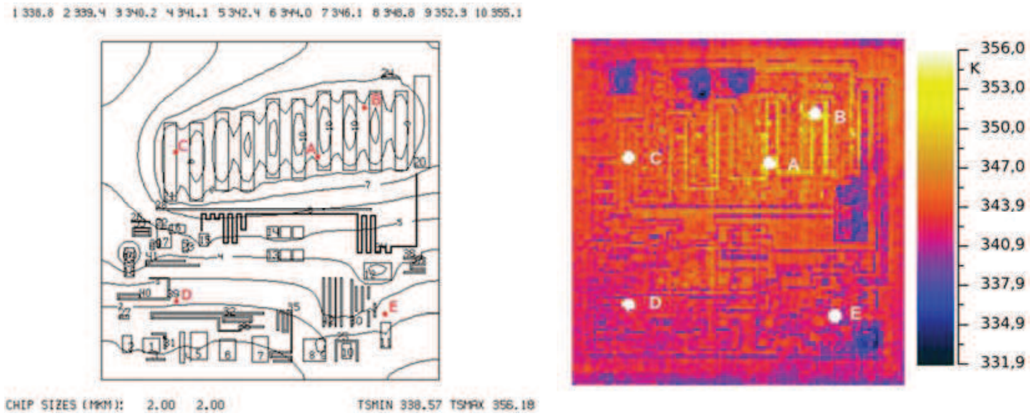
Right and inverse discrete Fourier transformations are calculated by means FFT - algorithms [7]. Using of this algorithms results in considerable decreasing of calculating time as compared with algorithms based on summation of Fourier series [8]. It is necessary to increase the difference network for the extension of calculation accuracy. This is not restriction for contemporaneous computers.

This algorithm we realize in the program “Overheat” for IBM PC [9]. The program allows to calculate both arbitrary heat regime of IC using the element powers and circuit layout as input data, and heat conductances, heat resistances and heat capacitances. The calculation of single heat regime requires 2 sec., using IBM PC Intel Core I7.

Modeling Results

The thermal calculation of power integrated voltage stabilizer was carried out by means of this method. It is fabricated by standard bipolar IC technology on 200 μm *h*-substrate with ρ_{sub}=10 Ω·sm and epi-layer ρ_{epi}=3 Ω·sm, d_{epi}=12 μm. Characteristics of this stabilizer is as follows: output voltage is U_{out}=20 - 40 V, output current is I_{out}=1 - 2 A.

The circuit operates reliably if its overheat not exceed 150 ^{0}C. The heat protection and power protection are used in the stabilizer for restriction the overheat.



a) b)

Figure 2. Temperature distribution on the voltage stabilizer 142EN9 chip surface.
a) simulated with Overheat, b) measured with FLIR A40 IR camera.

The two-dimensional temperature distribution on the top surface of semiconductor chip is shown Fig. 2a. This result is obtained using Overheat - program. The measured temperature distribution along the IC chip surface (see Fig. 2b) was obtained with FLIR A-40 IR camera. A good agreement between the measured and simulated 2D temperature distributions can be seen.

Electrical and Thermal Fields Modeling in Transistors of Integrated Circuits

The Mathematical Model of Integrated Transistors

As mentioned above, diffusion region thickness is much less than its layout sizes. Therefore, the electric field distribution in these regions is described by the two-dimensional equation:

$$\frac{\partial}{\partial x}\left[\rho_{\xi}^{-1}\frac{\partial U_{\xi}}{\partial x}\right]+\frac{\partial}{\partial y}\left[\rho_{\xi}^{-1}\frac{\partial U_{\xi}}{\partial y}\right]=j_{\xi}\left(x,y,U_{\xi},U_{\zeta}.T\right), \tag{13}$$

with the corresponding boundary conditions; where: x,y – co-ordinates of transistor layout, j_ξ – current density injected in region, ρ – sheet resistivity, U_ξ, U_ζ - this and other region, ξ, ζ – type of diffusion region, T – temperature, $\vec{n}$ - normal vector to boundary, U_{CONT} – potential of contact.

The thermal field model is similar described above.

Numerical Method

For simultaneous solution of heat transfer equation (Eq. 5)-(Eq. 9) and (Eq. 13) we use the simple iteration method. The heat transfer equation is solved by method described above. (Eq. 13) is solved by finite difference method, using the same grid, as for the (Eq. 5)-(Eq. 9). This nonlinear equation is solved by quasilinearization method along with successive over relaxation [10].

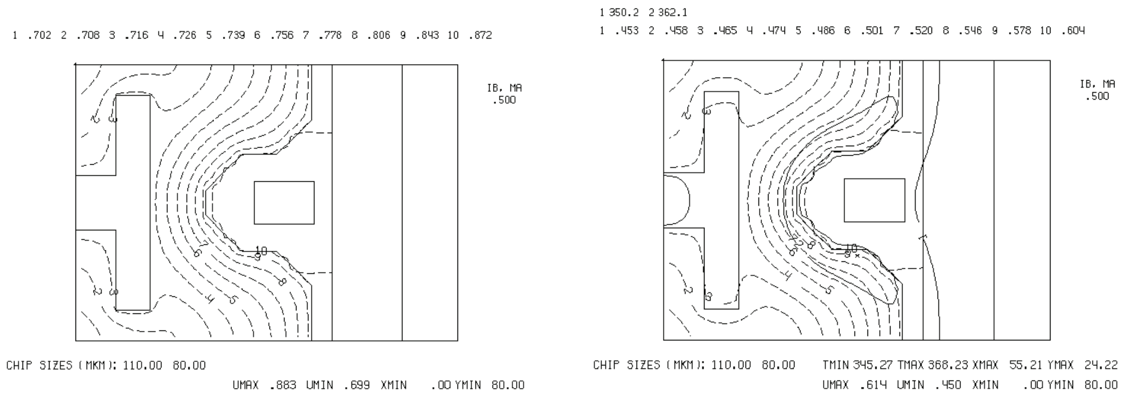
This algorithm was realized in the program “Selfheating” for IBM PC, [11]. The program allows to calculate arbitrary electro-thermal regime of IC transistors using its electro-thermal parameters and layout as input data. CPU time depends on the type of semiconductor device and varies from 1 min. to 10 min., using IBM PC Intel Core I7, for one point of electro-thermal regime. The similar simulations using 3D Synopsys model take 6 min. - 120 min.

Modeling Results

The electro-thermal calculation of power integrated bipolar transistor structure which consists of 58 uniform sections of the H-shaped form was carried out by means of this method, see Fig. 3 a,b.

Calculations of the electric mode of one cell of the transistor for base current of one cell I_B=0.5 mA and the collector - emitter voltage U_{CE}=10 V were made. This mode corresponds to the maximum output current of the circuit. First, the mode without self-heating for room temperature T=300 K is calculated, thus, base –emitter voltage U_{BE}=0.883 V is received as a result, see Fig. 3 a. Second, the mode with taking into account self-heating, thus, base –emitter voltage U_{BE}=0.614 B and T_{MAX}=368 K are received as a result, see Fig. 3 b.

The carried-out analysis shows strong dependence of the electric mode on the self-heating effect.



a) b)

Figure 3. The electro-thermal regimes of high power transistor structure with H-base region configuration.
a) The electric field distribution in the base region in the isothermal mode, I_B=0.5 mA, U_{BE}=0.883 V.
b) Distributions of electric field in the base region and temperature on a chip surface in non-isothermal mode, T_{MAX}=368 K, I_B=0.5 MA, U_{BE}=0.614 V.

Summary

The key point of quasi-3D approach for electro-thermal modeling of microelectronic devices based on the factor that the fully 3D problem is reduced to the set of 2D equations for different constructive layers of the device. It allows to reduce the three-dimensional equations of electric field and heat conductivity to systems of the two-dimensional equations that significantly simplifies a task. In other cases the analytical solution of the heat conductivity equation is applied. The considerable reduction of SPU time is attained. The acceptable accuracy of modeling is assured.

The possibilities of quasi-3D approach are illustrated at the electro-thermal modeling of power bipolar transistor and IC of voltage stabilizer.

This method was also used for: electro-thermal simulation of 4.5 Watt operational amplifier [12]; differently power transistors [13]; for smart power ICs temperature sensors modeling [14]; logi-thermal analysis of digital circuits [15], thermal modeling of hybrid IC and BGA packages. [16].

Authors developed the software realizing these approaches.

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