The Method of Automated Synthesis of Thermal Control Systems of Microelectronic Devices

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***Abstract* — This paper presents a description of the method of automated parametric and structural optimization of systems for ensuring thermal regime of microelectronic devices using modern information technologies.**

Keywords — microelectronic devices; optimization; design; automation; thermal regime.

I. INTRODUCTION

Modern microelectronic devices are characterized by complexity of embodiment, continuous miniaturization, as well as the growth of the density of dissipated thermal power. Thus, the reliability requirements remain extremely high. Consequently, the problem of optimal design of structure and parameters of thermal control systems (TCS) for the microelectronic devices becomes nontrivial, extremely difficult, or impossible for the optimal solution by an intuitive approach [1].

In this paper we propose methods and models to automate the selection process both tools of temperature control, and thermostatting for microelectronic devices and their parameters.

In most sources, first and foremost, it is the issue of parametric optimization of thermal systems that is considered [2]. The problem of simultaneous structural optimization, as a rule, is reduced to an iterative search for a simple comparison of various thermal control systems [3] which is time-consuming and inefficient when calculating complex models of microelectronic devices. The implementation of a fundamentally different approach to the synthesis of these systems based on an assessment of the effectiveness of the impact of TCS parameters on the thermal regime is given below.

To fulfill the requirements for thermal conditions of each electronic component, different tools of thermoregulation can be used [4]: local heat sinks, fans, heat sink buses, Peltier modules [5], heat pipes [6, 7], etc., which are combined in TCS structure associated with each cooled electronic component or microelectronic device structure element. An example of a thermal model of microelectronic device element and substitution options in the thermal circuit is shown in Fig. 1. On the scheme at fig. 1 heat flow from microelectronic components are modelled by current sources *Ie1-Ie9*, thermal resistance between them including board packet parts – by resistors R5,6,9,15,16,18,19,20,21,23,24,25, device housing wall – by R7, environment air temperature – by voltage source V1, convection from housing and components to air – by other resistors. Convection resistors at the scheme can be replaced by vary TCS tool thermal models, such as thermoelectric module Peltier, heat pipe set, heatsink and other in an TCS optimal configuration search process.

II. OPTIMALITY CRITERION

As a heat transfer model of microelectronic devices block, in the process of optimal synthesis, a heat balance made according to the principles of electrothermal analogy is used (Fig. 1). The concept of optimization method is based on the analysis of the temperature field, calculated according to the heat transfer model after step change of TCS parameters. When determining the direction of movement to the optimum the change of value of each parameter is determined by calculating at the next step of optimizing the optimality criterion for the microelectronic devices block, and the optimal direction of the parameter change for each TCS tools present in the model.

The criterion reflects the effectiveness of TCS configuration in the form of the interdependence of the cost of implementation and the resulting thermal effect. At the same time, the cost of implementation is the sum including the cost of TCS, their weight, and power consumption; the resulting effect is referred to reduction of the temperature deviation in the electronic components from the set points needed to ensure the required reliability.

To implement the above-mentioned interdependence, as an optimality criterion for the microelectronic devices block, it is proposed a minimum of the objective function F for n thermal control tools and m provided temperatures in electronic components at the nodes of the thermal model:

$$
\begin{aligned}
F(Q) = {} & \left(\sum_{i=1}^{n} C_i + \lambda_p \sum_{i=1}^{n} c_{p,i} P_i + \lambda_{м} \sum_{i=1}^{n} c_{м,i} M_i \right) \cdot \\
& \cdot \left(\lambda_l \sum_{ni=1}^{ne} \left(T_{ni} - k_{l,ni} T_{cl,ni} \right)^2 + \lambda_h \sum_{ni=1}^{ne} \left(T_{ni} - k_{h,ni} T_{ch,ni} \right)^2 \right),
\end{aligned}
\tag{1}
$$

where: $Q = (q_1, ..., q_u)$ – parameter vector of elements of the system with constraints (thermal resistance, power consumption, parameters of the wick for heat pipes, supply current for Peltier module, etc.); u – total parameters count from all TCS tools in the model; n – the number of nodes with individual TCS tools; i – an individual TCS tool node index, where will it be replaced by other possible; *ne* – number of thermal controlling electronic components; *ni* – index by nodes with thermal controlling electronic components; λ_l, λ_h, λ_p, $\lambda_м$ – weight coefficients of importance to consider requirements for the lower and upper values of temperature of electronic components, power consumption, and weight, respectively; $c_{p,i}$, $c_{m,i}$ – weight and mass coefficients for TCS tool in node *i*; $k_{l,ni}$, $k_{h,ni}$ – reserve coefficients (temperature) in node *ni* from 0 to 1 (from 0% to 100% of reserve); T_{ni} – calculated from model temperature for electronic components in *ni*-th node of the thermal model; $T_{cl,ni}$, $T_{ch,ni}$ – the lower and upper permissible temperature of *ni*-th electronic component; P_i – power consumption of TCS tool in *n*-th node; M_i – weight of the TCS tool; C_i – cost of the *i*-th tool.

Depending on the selected method for optimizing, penalty functions taking into account the restrictions on the vectors *Q* and *T* are added to the objective function.

It is required that the chosen solution was the most appropriate in terms of the cost of the use of certain tools of TCS. In this regard, an important feature of the proposed method is the possibility of taking into account the appropriateness of certain tools of TCS. This is achieved by taking into account the individual expert and the price parameter such as the value which characterizes the costs of the application. TCS costs (*C*) are generally specified as [8]:

$$C = f(Q). \tag{2}$$

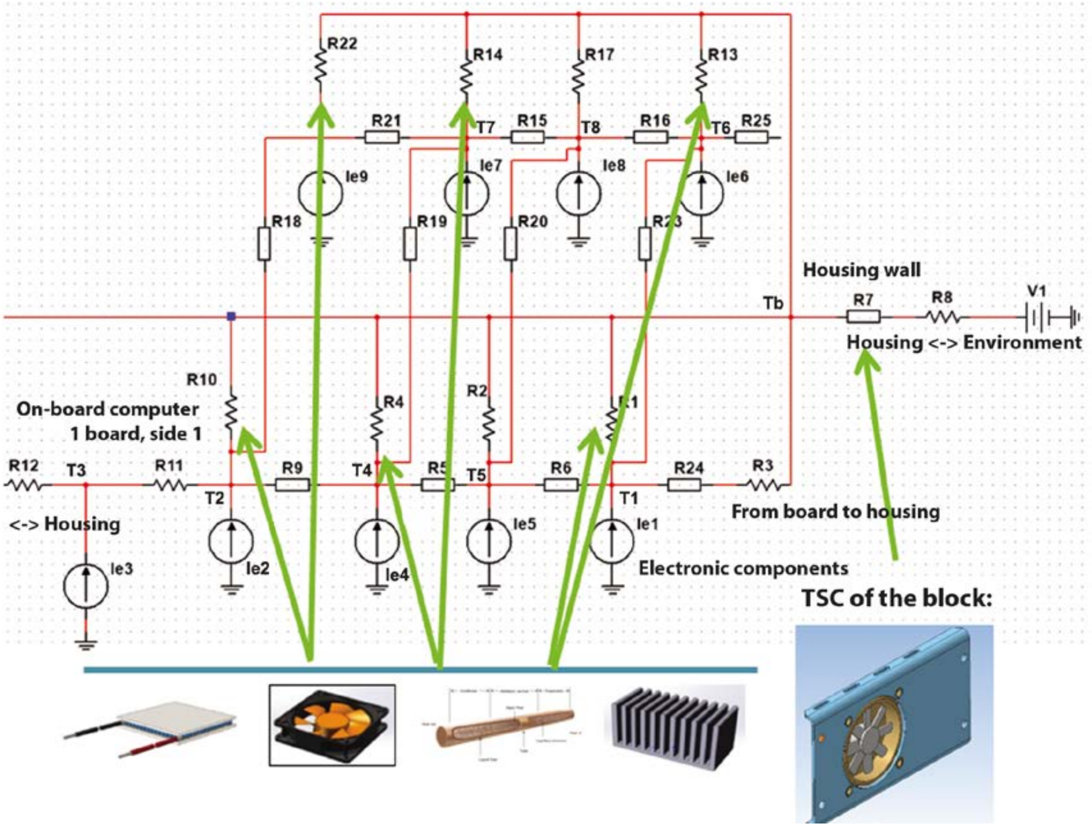

Fig. 1. Circuit of TCS substitution in the thermal model of microelectronic devices block

In practical optimization, *C* is represented in the form of a linear or polynomial function, examples of which are presented in chapter 5.

III. DESCRIPTION OF THE SYNTHESIS METHOD

Synthesis of tools of thermal control involves structural and parametric optimization. The proposed method is carried out to find the most effective tools of TCS as well as substitution of its electro-thermal analogue in the thermal model in the automatic mode. This process is inextricably linked with the search for optimal parameters of all elements of the thermal circuit. In the process of synthesis, configurations are created with the use of possible variants of TCS tool replacements in nodes. The efficiency of the configuration is evaluated using objective function (1).

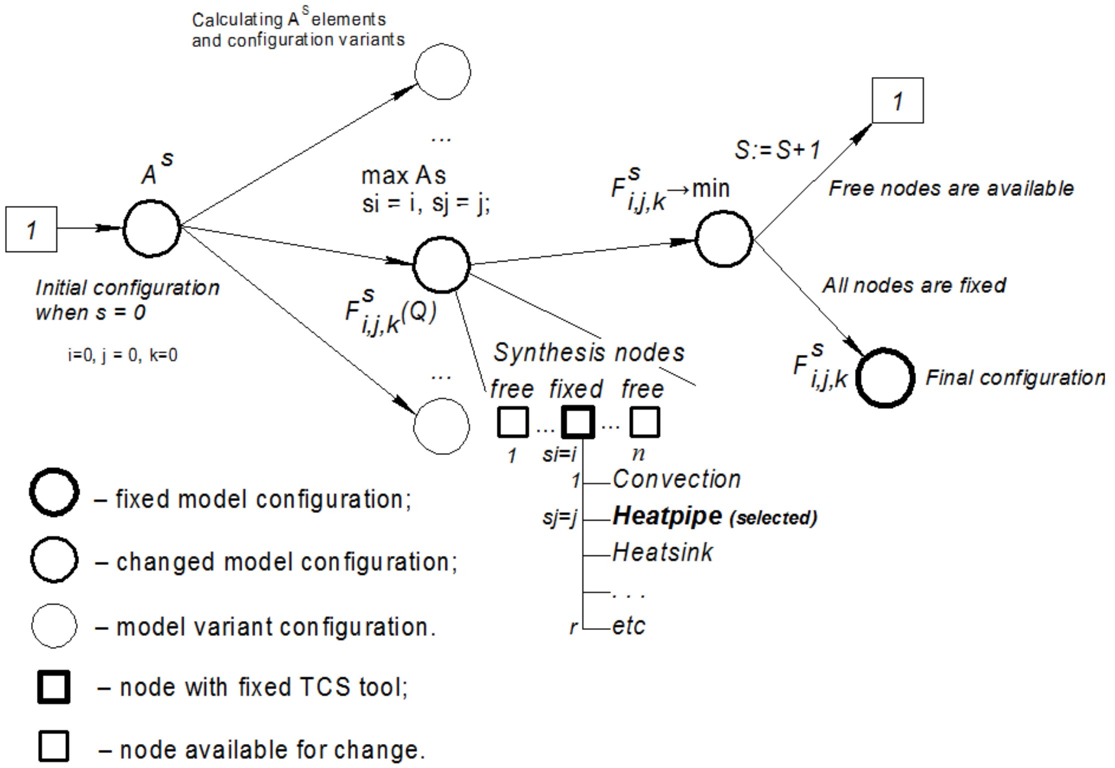

Fig. 2. Synthesis method basic steps and TCS configuration change example

The synthesis method is determined by the following basic steps (fig. 2):

Step 0. Initialization stage. Steps counter $S = 1$. In the initial configuration of the thermal model, for each synthesized node, the specialist assigns possible replacement options, or automatically considers all possible ones. Restrictions for F (1) and safety factors are assigned.

Step 1. Performing a search through the substitution nodes and calculating the matrix A^S. The state estimation of possible configurations of the synthesized model at the current optimization step S is performed using a matrix A^S with $n \times r$ size whose gm elements are the maximum values of a g vector:

$$A^S = \begin{bmatrix} gm_{1,1} & .. & gm_{1,r} \\ .. & .. & .. \\ gm_{n,1} & .. & g_{n,r} \end{bmatrix};$$

$$gm = \max(g_{1,1,1} \quad .. \quad g_{i,j,k} \quad .. \quad g_{n,r,p});$$

where: n –nodes count witch TCS tools search from available variants, r – maximum number of TCS tool that can be applied to search nodes, p – maximum available parameters in TCS tools; i, j, k – counters for search nodes, TCS tools in nodes, and TCS tool parameters, respectively.

The evaluation of the effect of each parameter of the TCS tool of the model is performed using the relative sensitivity of the objective function to the change of TCS tool parameter value and the absolute sensitivity of the cost of the TCS tool to the change of this parameter:

$$g_{i,j,k} = \left(\frac{\dfrac{q_{i,j,k}}{F_{i,j,k}} \cdot \dfrac{\partial F_{i,j,k}}{\partial q_{i,j,k}}}{\dfrac{\partial C_{i,j,k}}{\partial q_{i,j,k}}} \right),$$

where: $F_{i,j,k}$ – objective function (1) value in a point Q with $q_{i,j,k} \in Q$; $C_{i,,j,k}$ – a j-th TCS tool cost in search node i-th for k-th parameter; $q_{i,j,k}$ – a k-th parameter value in the point.

Step 2. Search for i, j of an A^S maximal element from. Assign $s_i = i$, $s_j = j$. A TCS tool with indices s_i, s_i is placed into the model and the node $n = s_i$ is marked as fixed in the matrix H:

$$H = \begin{bmatrix} h_1 \\ .. \\ h_n \end{bmatrix}, \quad h = \begin{cases} 0 \\ 1 \end{cases},$$

where h_i equals 0 for i-th node, if it's fixed, or 1 otherwise.

Step 3. Parametric optimization of the function (1) $F_{i,j,k} \to \min$ is performed in the fixed node i on the selected

TCS tool parameters by any well-known optimization method, taking into account the constraints, for example, by the method of steepest descent.

The process of finding a configuration with the estimation of the matrix A^S, selecting the TCS tool for the next node and fixing it from the changes continues until all the nodes of the synthesized circuit are fixed and $H = (0, ..., 0)$.

Step 4. S = S + 1. Checking $H = (0, \dots , 0)$?

True → Step 5

False → Step 2.

Step 5. Output of the final configuration, a list of selected TCS tools, electronic components and thermal model nodes temperatures.

It should be noted that when synthesis of the thermal circuit takes place, the substitution nodes of a TCS tools may not coincide with the one being substituted. For example, the components of heat flow to exit from the radiator to the atmosphere may not coincide with the release of the heat pipe which is output, as a rule, on the housing or the heat-removing element. Such configuration nuances must be considered in preparing the initial data, otherwise the synthesized thermal model and its intermediate states will be incorrect.

Structural synthesis is performed in the process of parametric optimization by eliminating inefficient tools of TCS compared with more efficient ones in order to achieve the minimum objective function.

IV. OPTIMAL TCS SYNTHESIS OF TYPICAL MICROELECTRONIC DEVICES BLOCK

Consider the optimal TCS synthesis of typical microelectronic devices block for which it is necessary to evaluate the appropriateness of the use of aluminum radiators on the electronic components compared with copper heat pipes whose condensation zones are output to the block housing. Included in the microelectronic devices block printed circuit boards have 6 key electronic components with heat value from 2 to 10 W.

Input data and boundary conditions:

- the atmosphere inside and outside of the block – air;
- thermal load – 6 electronic components with heat emission equal 2, 1.2, 1.5, 1, 0.8, 0.4 W (see *Ie1-Ie8*, fig. 1), respectively;
- heat pipes arranged horizontally with respect to the gravitational field, i.e. slope angle $\psi = 0$.
- the boundary conditions on the housing – the atmospheric temperature $T_a = 30$ °C;
- housing heat transfer coefficient on the air $\alpha = 2$ W/m^{2}K.

The applied cost function for radiator TCS tools:

$$C = 0{,}5\frac{D_l}{D_{l,\min}} + 0{,}2\frac{H_r}{H_{r,\min}} + \\ +0{,}3\frac{(N_r \cdot D_{elr} + N_r \cdot D_{elp} - D_{elp})}{(N_{r,\min} \cdot D_{elr,\min} + N_r \cdot D_{elp,\min} - D_{elp,\min})}. \qquad (6)$$

The applied cost function for heat pipe TCS tools:

$$C = 0{,}1\cdot\frac{D}{D_{\min}} + 0{,}8\cdot\frac{w}{w_{\min}} + 0{,}1\frac{Q_p}{Q_{\min}}\ \cdot \qquad (7)$$

In (6, 7), parameters for the radiator: D_l – the length of the finned surface; H_r – the height of the fin; N_r – the number of fins; D_{elr} – fin thickness; D_{elp} – clearance between the fins; $D_{l,min}$, $H_{r,min}$, $N_{r,min}$, $D_{elr,min}$, $D_{elp,min}$ – their minimum possible values, respectively; for the heat pipes: D – outer diameter of the heat pipes, w – thickness of the wick, Q_p – the calculated transmitted power, d_{min}, w_{min}, Q_{min} – minimum possible values of the above parameters, respectively.

Tables 1, 2, 3 presents the initial values and limits of varying for the parameters of the tools of optimized TCS.

TABLE I. BASIC PARAMETERS OF PLATE RADIATORS

Parameter name	**Initial value**	**Constraints**	**Variation**
H_r	200 mm	$10 \le H_r \le 300$	+
D_l	200 mm	$10 \le D_l \le 300$	+
D_{elr}	1 mm	$1 \le D_{elr} \le 4$	+
D_{elp}	2 mm	–	–
N_r	5	$5 \le N_r \le 12$	+
Material	*Al* (λ = 200 W/m·K)	–	–

TABLE II. VALUES OF INITIAL PARAMETERS OF THE HEAT PIPES IN THE SET

Parameter name	**Initial value**	**Constraints**	**Cost coefficient (c)**	**Variation**
D (outer diameter)	6 mm	$4 \le D \le 12$	0,9	+
w (thickness of the wick)	2 mm	$1 \le t_p \le (D\text{-}2)$	0,1	+
t_p (wall thickness)	1 mm	–	–	–
L_c (field width of condenser)	100 mm	–	–	–
L_e (field width of evaporator)	100 mm	–	–	–
L_a (length of the adiabatic section)	200 mm	–	–	–
Type of the wick	mesh	–	–	–
Housing material	*Cu* (λ = 401 W/m·K)	–	–	–
Material of the wick	*Cu* (λ = 401 W/m·K)	–	–	–
N (cellularity)	7870	–	–	–
d_s (wire	$6{,}25\cdot10^{-5}$ m	–	–	–

Parameter name	Initial value	Constraints	Cost coefficient (c)	Variation
thickness)				
ψ (slope angle)	0	–	–	–

TABLE III. PARAMETERS OF THE HEAT PIPE SET

Parameter name	Value	Constraints
Q_{min} (transmitted heat current)	equal Q_e = [2, 12] pitched 2	–
N_{max} (max number of heat pipes in the set)	5	$1 \le N_{max} \le 10$

There were 6 computational optimization sessions with different values of heat emission Q_e for the first electronic component (see *Ie1*, fig. 1) and fixed value of Q_e for the rest in order to study the algorithm optimization behavior for different input data.

As an optimality criterion for TCS of microelectronic devices block, the objective function corresponding to (1) was used. Constraints on the temperature in the nodes: $0 \le T_j \le 100$ °C. In the process of optimization, parameters of radiators and heat pipe diameters, and their quantity were varied using steps number 1-3 of the developed algorithm.

As a result of optimization, the algorithm proposed the final configuration in which electronic component #1 is cooled by the set of heat pipes, and the remaining electronic components – by the radiators, because the heat emission of the first electronic component is quite substantial, and its cooling with a massive radiator will lead to a jump in the cost and the value of the objective function, respectively (Table 4). The objective function minimization for different heat emission values Q_e by steps is shown on fig. 3. A *np* value and the parameter vector of each heat pipe in the set, required for the removing of the heat emission Q_e from the first thermostatic electronic component to the housing of the microelectronic devices block, are obtained. The parameters of the set of heat pipes and radiators, depending on the electronic component heat emission, are calculated.

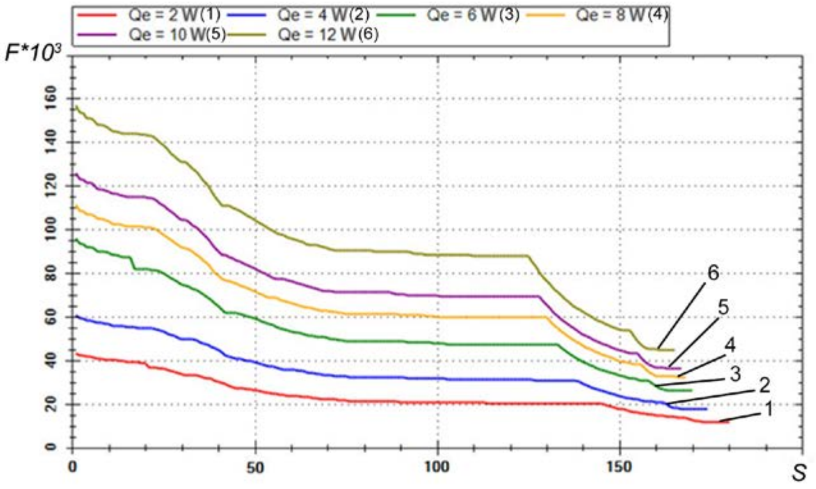

Fig.3. Dependence of objective function *F(Q)* on the optimization step *S* for different values of heat emission Q_e

TABLE IV. PARAMETERS OF THE SET OF HEAT PIPES FOUND BY OPTIMIZING

Q_{e1}, W	*np*	*D* HP, mm	Q_{max} HP, W	*R*, K/ W	*min F*
2	2	7,5	1,22	0,0207	11725,38
4	3	8	1,44	0,0202	17521,10
6	5	7,5	1,22	0,0207	26021,49
8	6	8	1,44	0,0202	32129,16
10	7	8	1,44	0,0202	36388,74
12	9	8	1,44	0,0202	44763,28

TABLE V. PARAMETERS OF RADIATORS FOUND BY OPTIMIZING, AS EXEMPLIFIED BY INDEX 2 ELECTRONIC COMPONENT

Q_{e2}, W	Parameters of radiator	*R*, K/W
0.2	D_l = 29 mm, H_r = 24 mm, N_r = 4, D_{elr} = 3 mm, D_{elp} = 2 mm	10,88
0.5	D_l = 32 mm, H_r = 27 mm, N_r = 5, D_{elr} = 3 mm, D_{elp} = 2 mm	8,74
0.8	D_l = 34 mm, H_r = 28 mm, N_r = 6, D_{elr} = 3 mm, D_{elp} = 2 mm	7,12
1	D_l = 39 mm, H_r = 30 mm, N_r = 6, D_{elr} = 3 mm, D_{elp} = 2 mm	4,15
1.5	D_l = 41 mm, H_r = 31 mm, N_r = 6, D_{elr} = 3 mm, D_{elp} = 2 mm	2,87
2	D_l = 42 mm, H_r = 33 mm, N_r = 6, D_{elr} = 3 mm, D_{elp} = 2 mm	1,7

As can be seen from Table 4, the algorithm found sufficient but not excessive amounts of heat pipes in the set *np* with diameter *D* for each value of Q_e. In each case, it is provided the minimum thermal resistance *R* of a single heat pipe in the set with the restrictions on the boiling and entrainment of the liquid, expressed in the calculated value of Q_{max} HP. Minimum value of the objective function (1) increases at the expense of increase in the cost of the use of the set with a large number of heat pipes in it.

The optimization algorithm proposed the parameters of radiators falling into the zone of restrictions and allowing performance of the temperature requirements for the electronic components on which they are installed. The usage of radiators is considered to be a classic and the simplest solution, from a technological point of view, but it requires a substantial increase in the size of the mainboard space of the microelectronic device; consequently, an increase in heat emission of the electronic components takes place, due to increased size of the radiator fins, which is clearly shown in Table 5.

TABLE VI. THE CALCULATED TEMPERATURES IN THE KEY NODES OF THE THERMAL MODEL

Q_e, W	***Tb***	***T1***	***T2***	***T3***	***T4***	***T5***	***T6***	***T7***	***T8***
	°C								
2	44,4	44,42	91,17	90,53	90,98	90,73	91,72	90,88	90,35
4	45	45,02	90,17	90,61	90,64	90,47	92,32	90,66	90,2
6	45,6	45,62	90,27	90,71	90,38	90,63	92,92	90,87	90,86
8	46,2	46,22	90,87	90,81	90,44	90,45	93,52	90,39	90,32
10	46,8	46,82	91,47	90,23	90,78	90,25	94,12	90,60	90,40
12	47,4	47,427	90,45	90,39	91,38	90,85	90,64	90,07	90,34

The calculated temperatures of thermostatically controlled, in this way, electronic components of the microelectronic devices block approach close to the upper limit, since optimization algorithm uses all possible resources to lower the cost of solution within the permissible limits of temperature (Table 6).

Table 6 shows the key components of the thermal model of the block. The nodes labeled as *T1-T8* (see fig.1) represent the point on the surface of the electronic components thermostatically controlled by the radiators, and *T1* – by the set of heat pipes; *Tb* – air temperature inside the microelectronic devices block in the hottest point. The change of the heat emissions Q_e of the first electronic component affects the temperature in the nodes of the entire model. At the same time, its temperature *T1* is minimal, because all emitted heat current is transmitted to the set of heat pipes and further to the housing of the block with minimal thermal resistance *R*, which shows the high efficiency of the heat pipes in TCS of the block in terms of the heat removal, but greatly affects the increase in the cost, that is shown in the value of the objective function (Table 4).

V. CONCLUSION

As a result, a method and a program of automated structural and parametric synthesis of the tools to provide the thermal modes of microelectronic devices were developed. The criterion of optimal design for assessing the effectiveness of the systems for ensuring the thermal regime based on expert-cost pricing was presented. The synthesis algorithm was designed, as well as the practical results, which allow confirming the effectiveness of this method, were obtained.

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