

An Enhanced Frequency Ratio Dual Band Balun Augmented With High Impedance Transformation

Rahul Gupta^{ID}, *Student Member, IEEE*, Mohammad S. Hashmi^{ID}, *Senior Member, IEEE*,
and Mohammad H. Maktoomi^{ID}

Abstract—Design of a dual-band balun achieving simultaneous high impedance ratio (> 20) and band-ratio (> 10) is reported in this brief. The presented design, augmented with closed-form design equations and a systematic design procedure, achieves excellent isolation between output ports and good matching at all the ports. A number of case studies are included to demonstrate the capability of the presented approach for varying design specifications and port-terminations. A prototype is developed for impedance transformation ratio (k) of 5 and frequency ratio (r) of 5 concurrently to evaluate the presented design approach show excellent agreement between the simulation and experimental results and thus validate the proposed design strategy. A comparative analysis with a number of recently reported dual-band impedance transforming components demonstrates superior performance of the proposed design.

Index Terms—Dual-band balun, high impedance transformation ratio, high frequency ratio, microstrip line, high isolation.

I. INTRODUCTION

MULTI-BAND baluns with inherent simultaneous high impedance transformation ratio (k), high frequency ratio (r), and isolation are extremely important to facilitate successful realization of advanced communication applications such as wireless power transfer, energy harvesting, RF front-end etc. [1], [2]. For example, for dual-band circuits the frequency ratio (r) refers to the ratio of second frequency (f_2) to the first frequency (f_1), and the impedance transformation ratio (k) refers to the ratio of load impedance (Z_L) to the source impedance (Z_S).

There exist numerous dual-band balun architectures capable of providing either high r or high k but very few reports discuss concurrent k and r . For example, [3] and [4] feature a dual-band balun with flexibility in the achievable frequency ratios but no impedance transformation, whereas a few recent dual-band balun designs do include analytical discussion on capability of dual-band baluns under different input and output impedance environments with some success [5]–[7]. The

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Rahul Gupta is with the Department of Electronics and Communication Engineering, IIT-Delhi, New Delhi 110020, India (e-mail: rahul@iitd.ac.in).

Mohammad S. Hashmi is with the School of Engineering and Digital Sciences, Nazarbayev University, Astana, Kazakhstan, and also with IIT-Delhi, New Delhi 110020, India.

Mohammad H. Maktoomi is with the School of Engineering and Computer Science, Washington State University, Vancouver, WA 98686 USA.

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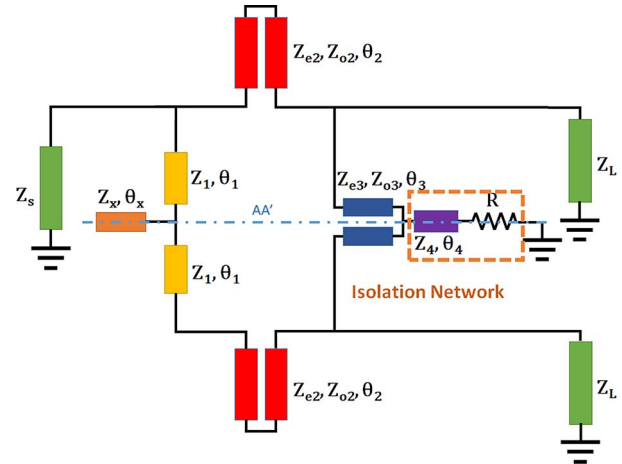


Fig. 1. Proposed dual-band balun architecture.

reported designs have although advanced the state-of-the-art in dual-band balun technology but there is still need of solutions for concurrently enhancing the r and k with information vis-a-vis k and r and their impact on the design parameters.

This brief, therefore, revisits the design of dual-band balun which is capable of achieving high k and high r simultaneously. In addition, the inherent port matching at all the ports and isolation between the output ports are also envisaged. The proposed design is based around a core of three coupled-line segments and also incorporates a simple isolation network to enable excellent isolation without increasing the design complexity. The odd- and even-mode analysis of the proposed architecture results in closed-form design equations which are then used to develop a systematic design procedure. The proposed design is supported by several design examples to comprehensively elaborate on the flexible design procedure, performance enhancement, and a prototype to demonstrate the performance in the dual-band balun state-of-the-art technology. In brief, the major focus of this brief is the design of balun with high r , high k , and concurrent high r and high k . The next section includes the odd- and even-mode analysis of proposed balun whereas Section III discusses features of the proposed balun under various operating conditions. The design procedure and the experimental evaluation and its comparison with recently reported dual-band balun and circuits employing impedance transformation are presented in Section IV. Finally, Section V concludes this brief.

II. PROPOSED ARCHITECTURE

The proposed dual-band balun shown in Fig. 1 has the source (input port) and the load (output ports) impedances

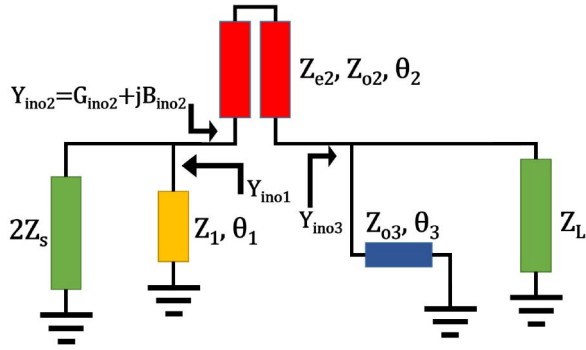


Fig. 2. Odd-mode equivalent circuit of the proposed balun.

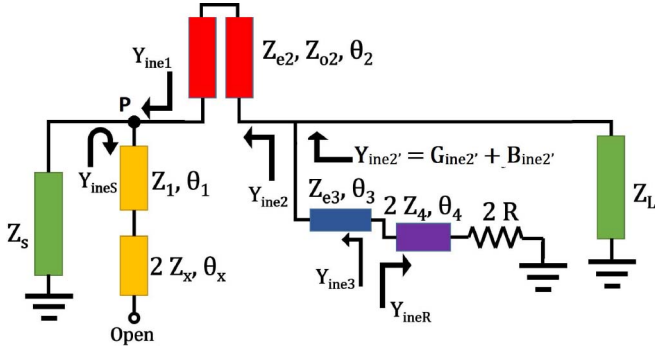


Fig. 3. Even-mode equivalent circuit of the proposed balun.

of $Z_S \Omega$ and $Z_L \Omega$ respectively. Here, all the electrical lengths are denoted by θ_i where $i = x, 1, 2, 3, 4$. Apparently the balun is symmetric around AA' axis (blue dotted line) in Fig. 1 and, therefore, can be analyzed using its equivalent odd- and even-mode circuits shown in Figs. 2 and 3 respectively.

The balun operates successfully if the conditions in (1) are met [8]. Moreover, the network consisting of a stub of electrical length θ_4 loaded with a resistor R is used to achieve isolation between the output ports. In addition, electrical lengths for dual-band designs are regulated by expression (2) [4]. Here, the term Z_{odd} is the odd-mode impedance at the input port, T_{even} is the transmission coefficient of signal in the even-mode, $r = f_2/f_1 \geq 1$, and $n \in \mathbb{Z}$.

$$Z_{odd} = 2Z_S \text{ and } T_{even} = 0 \quad (1)$$

$$\theta = \frac{(1+n)\pi}{1+r} \quad (2)$$

1) *Odd-Mode Analysis*: In the odd-mode equivalent circuit, Fig. 2, the transmission lines (TLs) with electrical length θ_1 and θ_3 are shorted to ground. Terms Y_{ino3} and Y_{ino2} in (3) and (4) can be deduced respectively. The subsequent expressions represent the terms in these expressions. It is important to note that all the electrical lengths are assumed equal, i.e., $\theta_1 = \theta_2 = \theta_3 = \theta$, for simplifications of these expressions.

$$Y_{ino3} = \frac{1}{Z_L} + \frac{1}{jZ_{o3} \tan \theta} \quad (3)$$

$$Y_{ino2} = G_{ino2} + jB_{ino2} \quad (4)$$

$$G_{ino2} = \left(Z_L Z_{o3}^2 (Z_{o2} \tan^2 \theta + Z_{e2})^2 / 4Z_L^2 \tan^2 \theta (A) \right) \quad (5)$$

$$B_{ino2} = (B - C) / (D + E) \quad (6)$$

$$A = \frac{Z_{e2}^2 Z_{o2}^2 + Z_{e2}^2 Z_{o2} Z_{o3} + \frac{Z_{e2}^2 Z_{o3}^2}{4 \tan^2 \theta} - Z_{o2}^2 Z_{e2} Z_{o3}}{\tan^2 \theta} - \frac{Z_{o3}^2 Z_{e2} Z_{o2}}{2} + \frac{4Z_{o3}^2 Z_{e2}^2 Z_{o2}^2}{Z_L^2} + \frac{Z_{o2}^2 Z_{o3}^2 \tan^2 \theta}{4} \quad (7)$$

$$B = \left(Z_{o2} \tan^2 \theta - Z_{e2} + 2Z_{o3} \tan^2 \theta \right) \cdot \frac{(2Z_{e2} Z_{o2} + Z_{e2} Z_{o3} - Z_{o2} Z_{o3} \tan^2 \theta)}{Z_{o3}^2 \tan \theta (Z_{o2} \tan^2 \theta + Z_{e2})^2} \quad (8)$$

$$C = 2Z_{e2} Z_{o2} \tan \theta (Z_{e2} - Z_{o2} \tan^2 \theta) / Z_L^2 (Z_{o2} \tan^2 \theta + Z_{e2})^2 \quad (9)$$

$$D = \frac{(2Z_{e2} Z_{o2} + Z_{e2} Z_{o3} - Z_{o2} Z_{o3} \tan^2 \theta)^2}{Z_{o3}^2 (Z_{o2} \tan^2 \theta + Z_{e2})^2} \quad (10)$$

$$E = 4Z_{e2}^2 Z_{o2}^2 \tan^2 \theta / Z_L^2 (Z_{o2} \tan^2 \theta + Z_{e2})^2 \quad (11)$$

The real and imaginary parts of Y_{ino2} are equated with $1/2Z_S$ and negative of Y_{ino1} to satisfy (1) respectively to get the design parameters Z_{o3} and Z_1 , expressed in (12), for given values of Z_{e2} and Z_{o2} . The terms Z_{e2} and Z_{o2} are independent variables here and can be chosen in the range of [20-160] Ω for the realizable Z_{o3} and Z_1 .

$$Z_{o3} = \frac{2Z_L Z_{e2} Z_{o2} (F)}{G} \quad Z_1 = \frac{H + I}{J - K} \quad (12)$$

where,

$$F = \sqrt{Z_S Z_L Z_{o2}^2 - \frac{2Z_{e2}^2 Z_{o2}^2}{\tan^2 \theta} + \frac{Z_S Z_L Z_{e2}^2}{\tan^4 \theta} + \frac{2Z_S Z_L Z_{e2} Z_{o2}}{\tan^2 \theta}} \cdot \sqrt{2} \pm \left(\frac{Z_L Z_{e2}}{\tan^2 \theta} - Z_L Z_{o2} \right) \quad (13)$$

$$G = -\frac{Z_L^2 Z_{e2}^2}{\tan^2 \theta} + 2Z_L^2 Z_{e2} Z_{o2} - Z_L^2 Z_{o2}^2 \tan^2 \theta + \frac{2Z_S Z_L Z_{e2}^2}{\tan^2 \theta} + 4Z_S Z_L Z_{e2} Z_{o2} + 2Z_S Z_L Z_{o2}^2 \tan^2 \theta - 4Z_{e2}^2 Z_{o2}^2 \quad (14)$$

$$H = \frac{(2Z_{e2} Z_{o2} + Z_{e2} Z_{o3} - Z_{o2} Z_{o3} \tan^2 \theta)^2}{Z_{o3}^2 (Z_{o2} \tan^2 \theta + Z_{e2})^2} \quad (15)$$

$$I = 4Z_{e2}^2 Z_{o2}^2 \tan^2 \theta / Z_L^2 (Z_{o2} \tan^2 \theta + Z_{e2})^2 \quad (16)$$

$$J = \left(Z_{o2} \tan^2 \theta - Z_{e2} + 2Z_{o3} \tan^2 \theta \right) \cdot \frac{(2Z_{e2} Z_{o2} + Z_{e2} Z_{o3} - Z_{o2} Z_{o3} \tan^2 \theta)}{Z_{o3}^2 (Z_{o2} \tan^2 \theta + Z_{e2})^2} \quad (17)$$

$$K = \frac{2Z_{e2} Z_{o2} \tan^2 \theta (Z_{e2} - Z_{o2} \tan^2 \theta)}{Z_L^2 (Z_{o2} \tan^2 \theta + Z_{e2})^2} \quad (18)$$

2) *Even-Mode Analysis*: The notations in even-mode equivalent circuit in Fig. 3 carry standard meaning. Here, condition in (1) can be satisfied by creating a virtual ground at the node P in Fig. 3, and this leads to $Y_{ine1} = Y_{ineS} = \infty$ for $\theta_1 = \theta_x = \theta$. $Y_{ineS} = \infty$ results in Z_x expressed in (19). Furthermore, the matching at the output ports can be achieved by enforcing $Y_{ineR} = Y_{ine3}^*$ [9] which can be solved to obtain Z_4 and R , given in (20) and (24), as functions of Z_{e2} , Z_{o2} , Z_{e3} , and θ . The independent design variable Z_{e3} in (29) can be calculated for the realizable coupling factor (ρ) while all the electrical lengths are assumed equal, i.e., $\theta_1 = \theta_2 = \theta_3 = \theta_4 = \theta$.

$$Z_x = \frac{1}{2} (Z_1 \tan^2 \theta) \quad (19)$$

TABLE I
DESIGN CASES FOR PROPOSED BALUN AT DIFFERENT FREQUENCY AND IMPEDANCE RATIOS (*: UNEQUAL ELECTRICAL LENGTHS)

Cases	r	k	Parameters												
			Z_1	θ_1	Z_X	θ_X	Z_{e2}	Z_{o2}	θ_2	Z_{e3}	Z_{o3}	θ_3	Z_4	θ_4	R
1	4.7	1	153.1	31.57	28.93	31.57	22	20	31.57	40.7	33.9	31.57	26.2	31.57	72.2
2*	10	1	55	49.09	36.62	49.09	42.4	32.9	49.09	121.1	100	49.09	32.5	16.36	78
3	2	8	31.9	60	47.9	60	140	110	60	168.6	80.3	60	29.7	60	39
4	2	20	20	60	29.3	60	140	110	60	196.7	93.7	60	22.75	60	49.6
5*	5	5	42.12	60	63.19	60	138.16	104.25	60	140.25	76.15	60	28.49	30	31.76
6*	6	4	25.01	51.43	19.67	51.43	50.45	45.86	51.43	131.75	116.63	25.71	70.88	25.71	32.99

B. Case Studies: Impedance Transformation Ratio

Once again all the electrical lengths are kept equal for various k , i.e., (Z_L/Z_S) and the design parameters are calculated. For example, Fig. 6 depicts that a balun with $r = 2$ is realizable upto $k = 20$ considering that all the design parameters are within the realizable limit as mentioned in case 4 of Table I. The plots in Fig. 7 convey that concurrent high k and r is also achievable using the proposed design though it comes with a trade-off where maximum achievable k is reduced to 2.2. However, unequal electrical lengths can support concurrent high k and r as mentioned in design examples in cases 5 and 6 in Table 1. As per authors' knowledge, baluns with such an ultra high k as well as concurrent high k and r are being reported for the first time.

C. Systematic Design Procedure

The design steps are summarised below:

- 1) Compute r and k based on specified frequencies of operations and port terminations Z_L and Z_S .
- 2) Calculate θ using (2), and choose the independent design variables Z_{e2} and Z_{o2} .
- 3) Then calculate Z_{o3} and Z_1 using (12). If any of these are not realizable then follow step-2 by keeping their realizability in perspectives.
- 4) If required, a higher value of n in (2) can be selected to satisfy the realizability of the design parameters.
- 5) Now, use (19) to calculate Z_X for the calculated Z_1 . If Z_X is not realizable then repeat steps 2 and 3.
- 6) Choose Z_{e3} and use (20) and (24) to calculate Z_4 and R . If Z_4 is not realizable then repeat step 5.

A number of cases and their corresponding design parameters are included in Table I to demonstrate the capability of the design for wide range of r and k . Cases 1 and 2 list the design example for high r while cases 3, and 4 provide design parameters for very high k . Case 2 is a design example with unequal TL. Design examples with concurrent high r and k are listed in Table I as cases 5, and 6. Once again, as per authors' knowledge, such concurrent high r and k are significant enhancement over existing state-of-the-art.

IV. ANALYSIS AND DISCUSSION

For experimental evaluation of concurrent high k and high r , case 5 from Table 1 is fabricated on RO5880 substrate with thickness of 1.57mm, ϵ_r of 2.2, loss tangent of 0.0009, and copper cladding of $35\mu\text{m}$ on both sides of the substrate. The design is simulated in Keysight ADS and the appropriate optimizations are done to account for the non-idealities of TL. The prototype, with the marked dimensions, along with the measurement setup, is depicted in Fig. 8. Here, Z_S is 50Ω and Z_L is 250Ω , and the design frequencies are 1.0/5.0GHz.

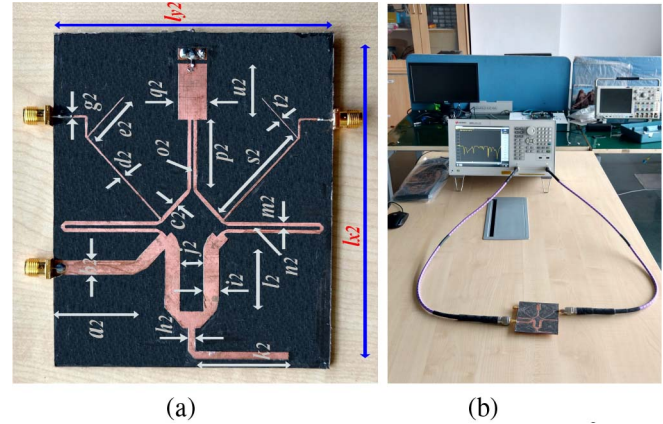


Fig. 8. (a) Fabricated Prototype with dimensions $101.4 \times 98.9 \text{ mm}^2$ and (b) measurement setup for $r = 5$ and $k = 5$. [$d_2 = 29.30$, $b_2 = 4.77$, $c_2 = 1.37$, $d_2 = 0.69$, $e_2 = 18.33$, $g_2 = 0.83$, $h_2 = 2.43$, $i_2 = 5.56$, $j_2 = 8.12$, $k_2 = 33.78$, $l_2 = 19.14$, $m_2 = 1.38$, $n_2 = 0.91$, $o_2 = 0.69$, $p_2 = 22.22$, $q_2 = 10.35$, $s_2 = 37.19$, $t_2 = 0.38$, $u_2 = 18.18$, $l_{x2} = 98.94$, $l_{x2} = 101.47$].

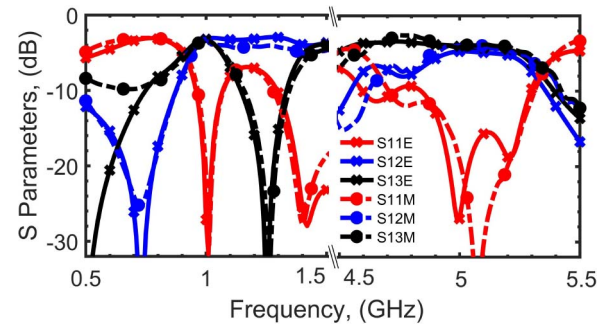


Fig. 9. EM Simulated vs Measurement results for S_{11} , S_{12} , and S_{13} , E: EM simulation results and M: Measurement Results.

Additional impedance transformers at the output ports create 50Ω environment for measurement purposes though at the cost of increased board size. The prototype is much smaller without these additional impedance transformers which are part of measurement infrastructure.

The measured and EM simulated results are compared in Figs. 9-11. The results in Fig. 9 demonstrate excellent matching at the input port. The measured (simulated) return loss is smaller than -30dB (-26dB) at both the design frequencies and the 10dB matching bandwidth is better than 110MHz @ 1GHz (11%) and 600MHz @ 5GHz (12%). These bandwidths readily meet the requirements of practical applications such as IEEE 802.11b/g/n (2.412-2.472 GHz, 2.5%), IEEE 802.11j (4.9-5.0 GHz, 2%), and narrowband IoT. The measured (simulated) insertion loss S_{21} is -3.66dB (-3.20dB) @

TABLE II
COMPARISON WITH STATE-OF-THE-ART BALUNS WITH HIGH FREQUENCY AND IMPEDANCE TRANSFORMATION RATIOS

[Ref]	r (f_1/f_2) (GHz)	k (Z_L/Z_S)	S_{11} (dB)	S_{21} (dB)	S_{31} (dB)	S_{23} (dB)	Percent Bandwidth (S_{11})	Phase Deviation (deg)
[5]	1/2.6	Exist but prototype uses $50\Omega/50\Omega$	<-16	-3.5/-3.8	-3.5/-4	<-21	29.7%/10.5% (<-10 dB)	3.0/0.5
[10]	1.0/5.0	NA	-36/-31	-3.24/-3.68	-3.24/-3.68	-29/-32	40%/5.71% (<-10 dB)	0.9/0.8
[6]	0.5/3.65	$100\Omega/130\Omega$	-37.5/-16.3	-4/-3.7	-3.7/-4	-26/-32.5	13.9%/2.8% (<-15 dB)	1.5/3.0
[7]	2.39/5.1	$150\Omega/50\Omega$	-36/-25	-3.46/-4.17	-3.45/-4.17	-28/-26	9.2%/4.5% (<-15 dB)	1.0/1.0
[This Work]	1.0/5.0	$250\Omega/50\Omega$	-29/-21	-3.6/-3.9	-3.4/-4.1	-25/-27	11%/12% (<-10 dB)	1.1/0.5

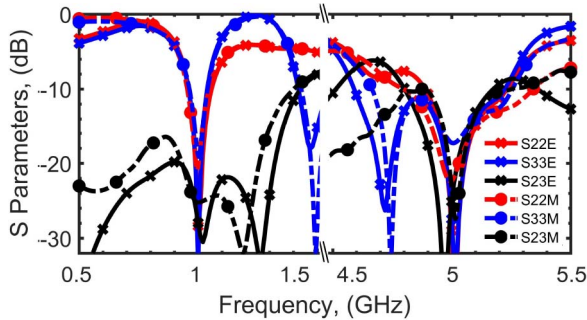


Fig. 10. EM Simulated vs Measurement results for S_{22} , S_{33} , and S_{23} , E: EM simulation results and M: Measurement Results.

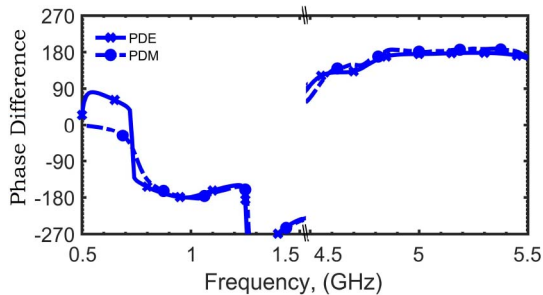


Fig. 11. EM Simulated vs Measurement results for Phase Difference (PD), E: EM simulation results and M: Measurement Results.

1GHz / -4.95dB (-4.75dB) @ 5GHz, and S_{31} is -3.44dB (-3.27dB) @ 1GHz / -4.17dB (-4.03dB) @ 5GHz. These results include the affect of redundant impedance transformers at the output ports. Furthermore, the output port matching and isolation are also promising as can be seen in Fig. 10. In addition, the amplitude and phase relationships between the output ports are depicted in Fig. 11. The measurement results are in good agreement with the EM simulation results. Overall, the presented design achieves very good performance in terms of isolation, matching, and bandwidth.

It is apparent from Table II that the design reported in [5] is terminated with 50Ω port impedances and hence not possible to understand impedance transformation ability. Another design [6] reports good performance at high r but is limited with k . A very recent balun architecture [7] demonstrates concurrent performance for $k = 3$ and $r = 2.13$ but at the expense of layout complexity considering the possibility of longer T-junction coupled line. The proposed design, on the other hand, possesses simple layout and exhibits favorable performance with significantly enhanced concurrent k and r , as

can be seen in the comparison Table II. As per authors' knowledge, these k and r are substantially higher as compared to the existing state-of-the-art. Therefore, it is safe to convey that the presented design advances the dual-band balun technology as it is capable of achieving simultaneous high k and r , exhibits excellent isolation between output ports, and possesses very good port matching.

V. CONCLUSION

A dual-band balun architecture with an integrated isolation network has been proposed in this brief. A thorough analysis results in closed-form design equations which help in the development of systematic design scheme. The proposed design achieves excellent performance specifically in terms of high k and r apart from very good isolation between output ports and matching at the ports. The proposed technique has been experimentally validated and a good agreement between measured and EM simulated is a testament to that.

REFERENCES

- [1] H. Lee, K. Kim, and B. Min, "On-chip T/R switchable balun for 5- to 6-GHz wlan applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 1, pp. 6–10, Jan. 2015.
- [2] S. Kim and K. Kwon, "A 50-MHz–1-GHz 2.3-dB nf noise-cancelling balun-lna employing a modified current-bleeding technique and balanced loads," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 2, pp. 546–554, Feb. 2019.
- [3] S. Y. Yang, C. S. Cho, J. W. Lee, and J. Kim, "A novel dual-band balun using branch-lines with open stubs," *Microw. Opt. Technol. Lett.*, vol. 52, no. 3, pp. 642–644, 2010. [Online]. Available: <https://onlinelibrary.wiley.com/doi/abs/10.1002/mop.24996>
- [4] A. L. Shen *et al.*, "Dual-band balun with flexible frequency ratios," *IET Electron. Lett.*, vol. 50, no. 17, pp. 1213–1214, Aug. 2014.
- [5] Y. Wu, L. Yao, W. Zhang, W. Wang, and Y. Liu, "A planar dual-band coupled-line balun with impedance transformation and high isolation," *IEEE Access*, vol. 4, pp. 9689–9701, 2016.
- [6] W. Zhang, Z. Ning, Y. Wu, C. Yu, S. Li, and Y. Liu, "Dual-band out-of phase power divider with impedance transformation and wide frequency ratio," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 12, pp. 787–789, Dec. 2015.
- [7] E. S. Li, C. Lin, H. Jin, and K. Chin, "A systematic design method for a dual-band balun with impedance transformation and high isolation," *IEEE Access*, vol. 7, pp. 143805–143813, 2019.
- [8] R. Gupta and M. Hashmi, "High impedance transforming simplified balun architecture in microstrip technology," *Microw. Opt. Technol. Lett.*, vol. 60, no. 12, pp. 3019–3023, Dec. 2018.
- [9] D. M. Pozar, *Microwave Engineering*, 3rd ed. Hoboken, NJ, USA: Wiley, 2005.
- [10] M. H. Maktoomi, D. Banerjee, and M. S. Hashmi, "An enhanced frequency-ratio coupled-line dual-frequency Wilkinson power divider," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 7, pp. 888–892, Jul. 2018.